ADVANCED MATERIALS AND PROCESSES FOR HIGH-DENSITY CAPACITORS FOR NEXT-GENERATION INTEGRATED VOLTAGE REGULATORS

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ADVANCED MATERISALS AND PROCESSES FOR HIGH-DENSITY CAPACITORS FOR NEXT-GENERATION INTEGRATED VOLTAGE REGULATORS

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS ..... **iii**

LIST OF TABLES ..... **vii**

LIST OF FIGURES ..... **viii**

LIST OF ABBREVIATIONS ..... **xiii**

SUMMARY ..... **xiv**

CHAPTER 1: INTRODUCTION **1**
- **1.1 Need for Integrated Voltage Regulators** **2**
- **1.2 Role of Capacitors in Integrated Voltage Regulators** **5**
- **1.3 Capacitor Materials and Processes to Date: Science and Technology** **7**
- **1.4 Capacitors in State-of-the-Art IVRs** **10**
- **1.5 Capacitor Requirements in Power Conversion and Distribution** **13**
- **1.6 Research Objectives** **15**
  - 1.6.1 Proposed Materials and Processes to Achieve Objectives 16
- **1.7 Technical Challenges and Research Tasks** **18**

CHAPTER 2: LITERATURE REVIEW **20**
- **2.1 Organic and Composite Laminate Films** **20**
- **2.2 Embedded Ferroelectric Films** **26**
- **2.3 Silicon Trench Capacitors** **30**
- **2.4 Etched Aluminum Films** **33**
- **2.5 Nanoporous Tantalum Capacitors** **34**
- **2.6 Summary of Prior Art** **36**

CHAPTER 3: CAPACITOR DESIGN **38**
- **3.1 Methods** **40**
  - 3.1.1 Capacitance Model 40
  - 3.1.2 ESR Model 50
  - 3.1.3 Capacitor Characterization and Measurements 52
- **3.2 Results** **53**
- **3.3 Discussion** **62**
- **3.4 Summary** **64**

CHAPTER 4: CAPACITOR FABRICATION AND PROCESS DEVELOPMENT **66**
- **4.1 Methods** **67**
  - 4.1.1 Anode Printing 67
  - 4.1.2 Dielectric Formation 70
  - 4.1.3 Cathode Deposition 73
  - 4.1.4 Electrical Measurement and Testing Methods 74
- **4.2 Results and Discussion** **74**
- **4.3 Summary** **82**

CHAPTER 5: 3D PACKAGE-INTEGRATION **83**
- **5.1 Methods** **84**
  - 5.1.1 Integration Process 84
  - 5.1.2 Electrical Measurements 89
- **5.2 Results and Discussion** **90**
- **5.3 Summary** **97**

CHAPTER 6: RELIABILITY EVALUATION AND MATERIAL COMPATIBILITY STUDY 98
6.1 Possible Degradation Mechanisms in Capacitor Materials....99
6.2 Evaluation and Testing Methods 104
6.3 Results and Discussion....107
6.4 Summary 117
CHAPTER 7: RESEARCH SUMMARY, CONTRIBUTIONS, AND FUTURE WORK 117
7.1 Research Summary 118
7.1.1 Capacitor Design....118
7.1.2 Capacitor Fabrication and Process Development....118
7.1.3 Capacitor Integration....119
7.1.4 Reliability Evaluation....120
7.2 Key Scientific and Engineering Contributions....120
7.3 Future Work....121
7.3.1 Cathode Infiltration Process Improvement....121
7.3.2 Alternative Cathode Materials....122
7.3.3 Continued Reliability Evaluation....123
7.4 Publications 123
7.4.1 Peer-Reviewed Journals....123
7.4.2 Conference Proceedings....124
7.4.3 Technical Reports....125
REFERENCES....126

LIST OF TABLES

Table 1. Summary of research objectives, challenges, and tasks 16
Table 2. Material properties of polymer dielectrics common in film capacitors [32] 22
Table 3. Dielectric constant (K), experimental band gap and (consensus) conduction band offset on Si various oxides [54] 31
Table 4. Summary of capacitor technology prior art and how it compares to proposed tantalum thin-film capacitors in this work 37
Table 5. Parameters used in capacitance and ESR model based on measurements obtained from an actual tantalum capacitor 56
Table 6. Comparison between capacitance of 5 mm^2 capacitors with an average nanoparticle size of 700 nm, measured using a liquid-electrolyte as the cathode versus solid PEDOT:PSS as the cathode 79
Table 7. Characteristics of low-profile solid tantalum capacitors from various manufacturers compared to the capacitors in this work 80
Table 8. Ability of tantalum capacitors to pass standard reliability testing methods for automotive qualification using MnO_2 versus polymer as the cathode material 101
Table 9. Summary of HAST reliability testing results with conditions of 65° C and 95% relative humidity 110
Table 10. Summary of reliability testing results of capacitors using 1000 nm thick Parylene C barrier layer coating following 335 hours at 85° C, 85% relative humidity, and 3.3 V DC bias 115

LIST OF FIGURES

Figure 1. Microprocessor trends over the past forty-two years from companies including IBM, Intel, AMD, etc. [6] 3
Figure 2. The benefits of integrated voltage regulation including (a) miniaturization of system, (b) reduced power supply line impedance, and (c) power savings from granular voltage regulation (Edited from [10]) 5
Figure 3. Schematic of a typical DC-DC buck converter using an inductor and capacitor, showing the effect of capacitance and inductance values on output ripple current 7
Figure 4. Schematic of a parallel plate capacitor comprised of two conducting electrodes separated by a dielectric material 8
Figure 5. Perovskite structure of BaTiO3 in (a) cubic phase [18] (b) tetragonal phase (c) orthorhombic phase [19]. In the non-cubic phases, the ability for titanium movement within the unit cell gives rise to ferroelectricity 9
Figure 6. (a) Epoxy-core inductor copper windings beneath PMIC (b) Top-view of surface-mounted MLCCs and inductor windings in Intel FIVR [21] 11
Figure 7. Integrated voltage regulator featuring embedded PMIC and surface mounted passives in a single package solution (a) Top-view photograph and (b) diagram of cross-section [22] 12
Figure 8. Proposed capacitor structure based on high-surface area, printed nanoporous films of tantalum 17
Figure 9. C-Ply high-permittivity laminate from 3M embedded in substrate [42] 22
Figure 10. PLZT-Polyimide composite-dielectric capacitor with (a) aerosol deposited PLZT ceramic dielectric and (b) self-healing ability of the dielectric film due to evaporation of Al electrode at defect site [41] 23
Figure 11. Enhancing performance of polymer film dielectric using multilayer structure [42] 24
Figure 12. High permittivity sol-gel dielectric with (a) polarizable side-chain structure (b) high permittivity and low loss up to 1 MHz and (c) minimal polarization hysteresis [43] 25
Figure 13. (a) Schematic and (b) cross-section of thin-film capacitors embedded in organic package. (c) Patterned electrodes connected to through-package via [47] 27
Figure 14. Reduced impedance due to TDK thin-film capacitors embedded in package [47] 28
Figure 15. Summary of technological developments leading to thinner BTO-based dielectrics [50] 29
Figure 16. Effect of grain size on dielectric constant for BTO for small grain sizes [39] 30
Figure 17. (a) Schematic of MIMIMIM trench capacitor (b) TEM image of TiN and Al_2O_3 layers at the bottom of the silicon trench capacitor [55] 32
Figure 18. High surface area tripod structures etched into silicon [53] 33
Figure 19. Embedded aluminum polymer capacitor from KEMET (a) cross-section (b) design targets [54] 34
Figure 20. Dependence of volumetric efficiency on component height in electrolytic capacitors using standard designs versus new ultra-thin designs [56] 35

Figure 21. Tantalum-pellet capacitor packaging options. The face-down undertab construction gives the best combination of volumetric efficiency and impedance characteristics [57].....35
Figure 22. (a) Approximated nanoparticle geometry before and after sintering (b) Branches of nanoparticles (anode) coated in conductive material (c) Equivalent circuit for basic unit of capacitor structure: a sintered nanoparticle coated in oxide and conducting polymer shells.....41
Figure 23. Equivalent RC ladder circuit of complete capacitor structure, with branches of sintered nanoparticles forming the RC ladder network within the nanoporous region of the capacitor.....44
Figure 24. (a) RC ladder circuit used in DC circuit simulation to evaluate capacitor charging characteristics, with a total of ten capacitor elements and tweny resistor elements (b) Comparison of the best-fit RC constants for each capacitor element predicted from simulation software to the RC constants calculated using Elmore's delay and branch capacitance methods (c) Comparison of the best-fit RC constants to the RC constants calculated using the hybrid method 48
Figure 25. Process flow for construction of capacitance and ESR model.....52
Figure 26. (a) Geometry used in FEA DC conduction simulations of tantalum-PEDOT:PSS nanoparticle-shell (b) Current density through cross-section of nanoparticle with Ta core radius of 122.5 nm and a 15 nm thick PEDOT coating, when a 3 V bias is applied across the ends of the nanoparticle (c) Effect of nanoparticle size and degree of sintering on nanoparticle resistance (c) Effect of PEDOT coating thickness and nanoparticle size on the coating resistance.....54
Figure 27. (a) SEM image of SEM cross-section of tantalum nanoparticle capacitor, with Ta foil anode terminal and graphite/silver paste cathode terminals below and above the nanoporous region of the capacitor (b) Internal nanoporous structure of capacitor populated with nanoparticles and pores (c) Various layers forming nanoparticle, with diameter and approximated overlapping spheres shown for the nanoparticles (d) Bottom of nanoporous region near Ta carrier foil, furthest from surface, showing very thin conducting polymer coating, if any. 57
Figure 28. Simulated and measured capacitor performance versus frequency, including (a) capacitance density and (b) ESR. All three methods for calculation of RC delay are included......58
Figure 29. Calculated relationship between RC time constant and nanoparticle distance from the upper surface cathode for the measured capacitor based on simulation results.....59
Figure 30. Predicted effect of PEDOT conducting polymer cathode thickness on (a) capacitance density and (b) ESR of a 50 μm thick, 300 nm core particle size tantalum capacitor, using the hybrid model to calculate the RC delays, where the 15 to 1 nm thickness represents a linear reduction in thickness from the surface nanoparticles to the most interior ones. Other than the PEDOT thickness, the model parameters are unchanged from Table 5. 60
Figure 31. Effect of the height of the nanoporous region in the capacitor on (a) capacitance density and (b) ESR (Inset: Effect of capacitor lateral area on ESR), assuming a conformal 15 nm thick coating of PEDOT on the nanoparticles. Other than the capacitor height or area and PEDOT coating thickness, the model parameters are unchanged from Table 5. 61

Figure 32. (a) Capacitance density versus frequency and (b) ESR versus frequency when 15 nm coatings of PEDOT or TiN is used as the cathode material. Other than the cathode material and thickness, the model parameters are unchanged from Table 5. 62
Figure 33. Thin-film tantalum capacitor fabrication process 67
Figure 34. Tantalum carrier foil with printed capacitor anode array consisting of 5 mm^2 regions of 50 µm thick, porous tantalum (enlarged SEM image showing sintered tantalum nanoparticles that populate the porous regions)....68
Figure 35. Experimental setup used for obtaining capacitance measurements of the tantalum capacitor array using a liquid electrolyte cathode 70
Figure 36. Proposed point defect model of tantalum pentoxide growth in an acidic electrolyte [72] 71
Figure 37. Experimental setup used for anodization of the tantalum anode and growth of amorphous tantalum pentoxide....71
Figure 38. (a) Current measured during anodization (a) ramp to formation voltage (0.005 V/s) and (b) anodization dwell....73
Figure 39. Anodization ramp (0.005V/s) using larger 700 nm tantalum particle size 73
Figure 40. (a) Tantalum nanoparticles comprising the capacitor anode (b) Oxide shell formed around the tantalum nanoparticles after anodization (c) Conducting polymer coating surrounding the particles after cathode dipping (d) Final cross-section of the capacitor structure after deposition of termination layers....75
Figure 41. Linear relationship between formation voltage and tantalum pentoxide thickness....77
Figure 42. Inverse power law relationship between formation voltage and volumetric capacitance density with (a) 285 nm tantalum particle size and (b) 700 nm tantalum particle size, considering only the volume of the 50-µm thick nanoporous region. When the entire capacitor thickness is considered, including the termination layers, the resulting volumetric density is roughly half of what is shown 78
Figure 43. (a) Volumetric capacitance density versus frequency of the thin-film tantalum capacitors compared to commercial surface mount tantalum capacitors, with the operating voltage included (b) Comparison of ESR for the same capacitors 80
Figure 44. Capacitance versus frequency for higher voltage tantalum thin-film capacitors with 700 nm particles and 5 mm^2 area....82
Figure 45. Summary of process used for package-integration of thin-film tantalum capacitors 84
Figure 46. Effect of UV laser power and pulse repetitions on depth of removed build-up material (Ajinomoto ABF GX92) at the drill site....87
Figure 47. Optical images of via bottoms after UV laser drilling for (a) cathode landing without gold stopping layer, with burning of silver paste visible; (b) cathode landing with gold stopping layer; (c) anode landing without gold stopping layer, with tantalum oxidation visible; (d) anode landing with gold stopping layer....88
Figure 48. Top-view optical images of (a) cathode via opening after copper sputtering (b) cathode via opening after copper electroplating (c) anode via opening after copper sputtering (b) anode via opening after copper electroplating....89
Figure 49. Cross-section of ~100 µm thick tantalum capacitor structure 91

Figure 50. (a) Thin-film Ta capacitor laminated and planarized on silicon (b) Thin-film capacitor after laser drilling of via and electroless copper deposition (c) Partially filled copper via contacting Au/silver paste cathode layers (d) Thin gold layer between copper via and silver paste layer for low resistance electrical connection 92
Figure 51. (a) Copper via interconnection to silver paste current collecting layer, electrically connected to conducting polymer coating on porous tantalum nanoparticles (b) Copper via interconnection to tantalum carrier foil, electrically connected to porous tantalum nanoparticles 93
Figure 52. Frequency characteristics of a capacitor array before and after capacitor integration, where the embedded capacitor measurements are taken through the copper vias (a) Capacitance vs. frequency (b) ESR vs. frequency 94
Figure 53. Distribution of leakage currents taken from a total of three separate arrays of ~10 µF capacitors 97
Figure 54. Depiction of the swelling of PEDOT:PSS cathode material caused by moisture absorption, leading to increased resistance and possible damage to the capacitor dielectric material 101
Figure 55. Schematics of how moisture absorption can lead to tantalum capacitor performance degradation including (a) increased capacitance at low frequencies due to increased area coverage of the tantalum nanoparticles but lower capacitance at higher frequencies due to increased resistance, leading to higher RC constants and larger roll-off (b) Increased conduction through the dielectric due to the accumulation and increased number of defects and (c) increased charge absorption losses from changes in band offset energy at the polymer-dielectric interface 103
Figure 56. Summary of possible degradation mechanisms in tantalum-polymer thin-film capacitors 104
Figure 57. PEDOT:PSS bridges used as test structure to study the effects of moisture and air on PEDOT:PSS morphology and electrical properties 105
Figure 58. (a) Testing set up used to connect the integrated capacitor arrays to the electrical outlets within the HAST chamber, where all of the capacitors are connected in parallel to an external voltage source (b) A picture of the HAST chamber used in this study 106
Figure 59. Relative change in resistance of PEDOT:PSS bridges with and without Parylene C barrier coatings after exposure to air at 120° C 107
Figure 60. Relative change in resistance of PEDOT:PSS bridges after exposure to 85° C and 85% relative humidity for various periods of time and with various Parylene C coating thicknesses 108
Figure 61. Effect of exposure to 65° C and 95% relative humidity on the frequency response of thin-film tantalum capacitors with a 200 nm Parylene C coating on (a) capacitance, after 500-hour HAST (b) ESR, after 500-hour HAST (c) capacitance, after 500 HAST (d) ESR, after 1000-hour HAST 112
Figure 62. Effect of extreme moisture absorption and oxidation on tantalum thin-film capacitors exposed to 85 % relative humidity and 125° C temperature for 100 hours on (a) capacitance and (b) ESR 113
Figure 63. Distribution of ESRs, measured at 100 kHz, from package-integrated capacitors exposed to 85° C, 85% relative humidity, and 3.3 V DC bias for 335 hours where (a) 500 nm thick Parylene C is used, (b) 700 nm thick Parylene C is used, and (d) 1000 nm thick Parylene C is used 114

Figure 64. Cumulative distribution of leakage currents for tantalum thin-film capacitors after fabrication (free-standing), after integration and via formation (embedded), and 335 hours of HAST at 3.3 V DC bias, 85° C, and 85% relative humidity (after burn-in) 116

LIST OF ABBREVIATIONS

AI	Artificial Intelligence
3D	Three-Dimensional
ABF	Ajinomoto Build-up Film
AC	Alternating Current
ALD	Atomic Layer Deposition
ASIC	Application-Specific Integrated Circuit
BET	Brunauer-Emmett-Teller
BOPP	Bi-axially Oriented Polypropylene
BST	Barium Strontium Titanate
BTO	Barium Titanate
CPU	Central Processing Unit
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DC	Direct Current
DF	Dissipation Factor
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FCC	Face-Centered Cubic
FEA	Finite-Element Analysis
FIVR	Fully-Integrated Voltage Regulator
GPU	Graphics Processing Unit
HAST	Highly Accelerated Stress Test
I/O	Input/output
IC	Integrated Circuit
IVR	Integrated Voltage Regulator
MIM	Metal-Insulator-Metal
MIMIMIM	Metal-Insulator-Metal-Insulator-Metal-Insulator-Metal
MLCC	Multi-Layer Ceramic Capacitor
PCB	Printed Circuit Board
PDN	Power Distribution Network
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) polystyrene sulfonate
PLZT	Lead Lanthanum Zirconium Titanate
PMIC	Power Management Integrated Circuit
RDL	Redistribution Layer
SEM	Scanning Electron Microscopy
SMD	Surface-Mounted Device
TFC	Thin Film Capacitor
TPV	Through-Package Via
UV	Ultraviolet

SUMMARY

Capacitors are the key components for power that includes conversion, stable power delivery, and power management. Along with inductors, they dictate the size and performance of voltage regulators in power distribution networks (PDNs) in electronic systems. Voltage regulators convert and regulate the power that gets delivered to the increasingly power-hungry processing integrated circuits (ICs). When the voltage regulators are integrated into the package, referred to as integrated voltage regulators (IVRs), they provide many benefits over traditional voltage regulators. These benefits include higher power density, system miniaturization, and improved efficiency. To enable IVRs, capacitors must be integrated either on-chip or in the package, while providing high capacitance density, high frequency stability, low equivalent series resistance (ESR), and high temperature stability. The focus of this thesis is design and demonstrate capacitors that can achieve these objectives by understanding the relationships between materials, process, and bulk capacitors properties.

Capacitors can be formed from a diverse range of materials. Tantalum capacitors have an advantage over many other types of capacitor material technologies due to their high capacitance density and high temperature stability. In these capacitors, the nanoparticle-based anode provides an ultra-high surface area, so that high volumetric capacitance densities can be achieved. A Ta_2O_5 dielectric can be formed directly on the anode structure to provide a high-permittivity oxide that is incredibly stable with changes in temperature. However, the high-surface area electrodes used so far result in long electrical pathways for charge and discharge current, which results in capacitors with high ESR and low frequency stability. Additionally, these capacitors are formed as pressed pellets, which means they are only available as bulky components that must be

surface mounted on the printed circuit board (PCB) rather than embedded into the package.

This research proposes a design and fabrication technologies to form innovative printed tantalum thin-film capacitors that solves many of the issues associated with traditional tantalum capacitors. The thin-film design results in capacitors with an ultra-thin form factor of just 100 μm in thickness. Additionally, the thin structure provides shorter pathways for the charge and discharge current, dramatically improving the frequency stability and reducing the ESR of the capacitors while maintaining ultra-high capacitance density.

The thesis starts by providing a background on the importance of IVRs and the role of capacitors in an IVR system. It then reviews of state-of-the-art and developing capacitor material technologies that may be compatible with IVR, while also understanding some of the challenges they face. After understanding the research objectives and prior art, a model is developed that is used to correlate the capacitor materials' nanostructures to the bulk device properties, including capacitance density, frequency stability, and ESR. A process is then developed to fabricate the capacitors, followed by their structural and electrical characterization. Next, a novel process is demonstrated to integrate these capacitors onto a package. The integrated capacitors are shown to meet the performance objectives set out for this work. Finally, evaluation of the capacitor reliability is conducted to ensure extended operation lifetimes of the capacitors at high temperatures, as would be the case in real high-power IVR systems. The research described here enhances materials science and engineering in many ways to accomplish the capacitor objectives:

1. A model is developed that provides insight into the relationship between material nanostructure and bulk device properties

2. The relationship between process, structure, and performance of the nanoporous tantalum anode, tantalum pentoxide dielectric, conducting polymer cathode, and packaging materials is studied
3. A greater understanding of the capacitor material degradation mechanisms is achieved, and a barrier material strategy is developed to limit the degradation and improve capacitor lifetime and high-temperature operation capability

CHAPTER 1: INTRODUCTION

The number of transistors on a semi-conductor chip has continued to double every two years according to a law made famous by Gordon Moore, also known as Moore's Law [1]. As a result, computing power has increased dramatically, enabling huge advancements in computationally-intensive technologies such as high-speed telecommunications, data processing, machine learning, artificial intelligence (AI), autonomous driving of fully electric vehicles, and virtual reality. This scaling of chip size and functionality has been accompanied by gradual improvements in input/output (I/O) density, power density, and component density to meet the needs of higher processing speeds.

While Moore's Law has continued to provide benefits to transistor scaling and performance, it is also beginning to slow down [2]. The benefits traditionally associated with transistor size reduction, such as reduced cost and improved performance, no longer hold true due to many issues such as device yield, increased design complexity, and disadvantages in electrical parameters such as power consumption and large on-chip signal delays [3]. Together, these issues result in increased costs and lower system performances. To continue pushing the limits of processing speeds at device and system levels, innovations must be made off-chip by the heterogeneous integration of multiple chips and other components into single, high-density packages. This second wave of system scaling will instead be led by innovations in the packaging and heterogeneous integration of devices and components in the system package [4, 5]. Achieving high signal bandwidth between devices in ultra-small form-factors has become a key driver for research and development in electronic systems packaging, and as a result, higher power densities are needed. This is driving new paradigms in component

integration for power delivery and distribution, 5G communications, sensor integration with wireless power and ultra-thin flexible packages, high-reliability electronics, and other applications. This thesis focuses on components for power conversion and distribution.

1.1 Need for Integrated Voltage Regulators

With continued advancements in redistribution layers (RDLs), 3D through-package vias (TPVs), or other high-density I/O technologies in electronic packages, the signal bandwidth continues to increase as it did with device scaling and is soon projected to reach up to TB/s or more. However, power delivery has remained a huge challenge in both mobile and high-performance computing systems. The transistors require power to operate, so, as the density of transistors on-chip increase due to transistor scaling, and the active component density increase due to package-scaling, so must the density of power being delivered to the devices and package (Figure 1). Thus, improved power distribution networks (PDNs) are needed to keep up with bandwidth scaling. Power delivery incorporates three elements: power storage, power conversion, and low-impedance power distribution to various domains in the IC. This thesis focuses on the second element, power conversion.

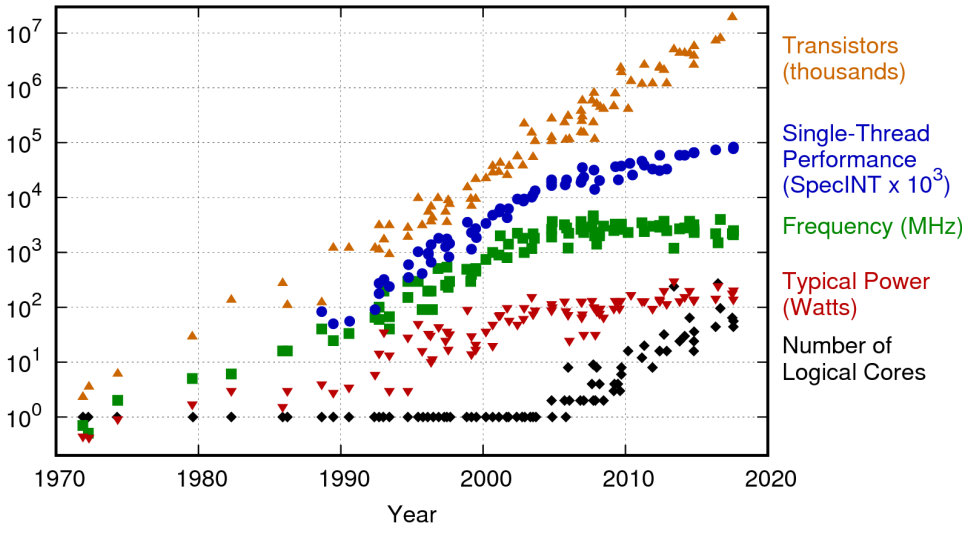


Figure 1. Microprocessor trends over the past forty-two years from companies including IBM, Intel, AMD, etc. [6]

Large complex chips demand high currents with low voltages and low noise margins. The ability to provide power to increasingly large, multicore processors quickly runs into area, efficiency, and thermal limitations that cannot be met by discrete, on-board voltage regulators because of two challenges [5, 7]. The first challenge is the significant power loss and Joule heating through the chip and package interconnects. Conversion of power from higher-voltage power sources, such as batteries, results in large currents traveling through the printed circuit board (PCB), package, and chip that resistively heat the system. Higher temperatures can be detrimental to the many materials and interfaces within the complex package and system. Single-stage power conversion with high voltage conversion ratios can allow the package power rails to run at higher voltages, leading to the best power efficiency, since most of the higher current levels are restricted to the chip.

The second challenge arises because the voltage noise budget is dominated by the inductive parasitics that reflect power and signal, requiring a complex network of decoupling capacitors to control the noise. To realize integrated voltage regulators

(IVRs), higher switching frequencies are generally required to reduce the total inductance and capacitance requirements by minimizing the AC ripple from the current in the system. The relationship between switching frequency (f_{sw}), output peak-to-peak voltage ripple (V_{pp}), output peak-to-peak current ripple (I_{pp}) and bypass (or decoupling) capacitance (C_{bypass}) in a DC-DC power converter is included in Equation 1.

$$V_{pp} \propto I_{pp} \propto \frac{1}{C_{bypass} f_{sw}} \quad (1)$$

A similar relationship holds true for the inductive components. Thus, there is a continuous movement in power supply switching from kHz to MHz due to the higher power densities and reduced capacitance and inductance requirements it enables [8, 9]. However, both the voltage regulator and the capacitors themselves must necessarily be capable of operating at these higher frequencies, which requires low parasitic resistance and inductance coming from package interconnect and the internal electrode materials of the capacitors.

In order to address both these two challenges, it is necessary to move the voltage regulator as close to the load as possible. The first and most obvious benefit is that this enables miniaturization of the entire system, and allotment of circuit board space for a greater number of components and functionality. Another benefit is that this minimizes the interconnect length throughout the PDN, so that both power losses and the need for decoupling capacitors, is minimized. As mentioned, impedance from longer interconnects becomes increasingly problematic at higher switching frequencies due to the reflected power and signal, so shorter interconnects through the PDN also help in this regard. Additionally, moving the voltage regulator closer to the load enables more granular power management. Fine-grain power management minimizes wasted energy from workload variability within a voltage domain, providing higher system efficiency. As heterogeneous integration of multiple chips continues, granular power management

becomes even more critical. With each of the multiple CPUs, memory devices, GPU, and other subsystems requiring their own voltage regulation, bulky voltage regulators placed on-board becomes incompatible with the area and volume constraints placed on the system. Figure 2 summarizes the benefits of using IVRs.

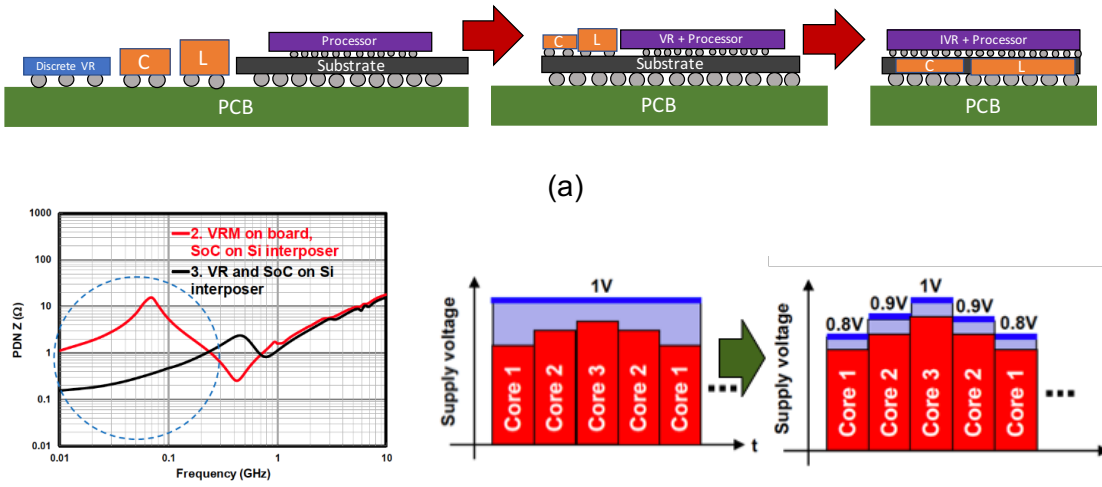


Figure 2. The benefits of integrated voltage regulation including (a) miniaturization of system, (b) reduced power supply line impedance, and (c) power savings from granular voltage regulation (Edited from [10])

1.2 Role of Capacitors in Integrated Voltage Regulators

Passive components, including both inductors and capacitors, pose a bottleneck for realizing a miniaturized and efficient IVR. Current on-board implementations do not allow for integrated voltage regulation due to their bulky size and distance from the active components. Again, this limits the switching frequency due to signal reflection, and thus the power density that can be achieved since a steady output voltage is required. To compensate for this, large, surface-mounted capacitors must be used according to Equation 1 to provide sufficient decoupling and thus a large amount of space must be allotted for them. However, the 3D integration of high-density passives embedded within the substrate provides the space savings and small interconnect

lengths needed for high-performance IVRs that can both switch as faster frequencies and provide steady output voltage at much higher power levels, all in an ultra-small form factor [11].

Additionally, capacitor-centric circuit topologies, such as the resonant switch-tank capacitor converter, can enhance the energy density of a power distribution system even further by minimizing dependence on bulky magnetics [12-17]. Capacitors can provide theoretically higher power density than inductive components, so high-density capacitors integrated closed to the switches and load can reduce the dependence on magnetics. A typical buck converter used commonly in PDNs as the final stage of power conversion is included in Figure 3. The input/output voltage conversion ratio is determined by the on/off time of the upper and lower switches, Q_1 and Q_2. During the on-time, the current rises as energy is stored in the magnetic field of the inductor, which is then released during the off-time at a different voltage than the input. The inductance value of the inductor needs to be large enough to mitigate the amount of current rising and falling that occurs over each period. However, any leftover ripple can be mitigated with the use of a decoupling capacitor at the output. Thus, by using larger decoupling capacitance, the inductance requirement can be minimized and higher conversion ratios, as well as higher power densities and higher conversion efficiencies, can be achieved. Therefore, the key focus of this research will be on the capacitor.

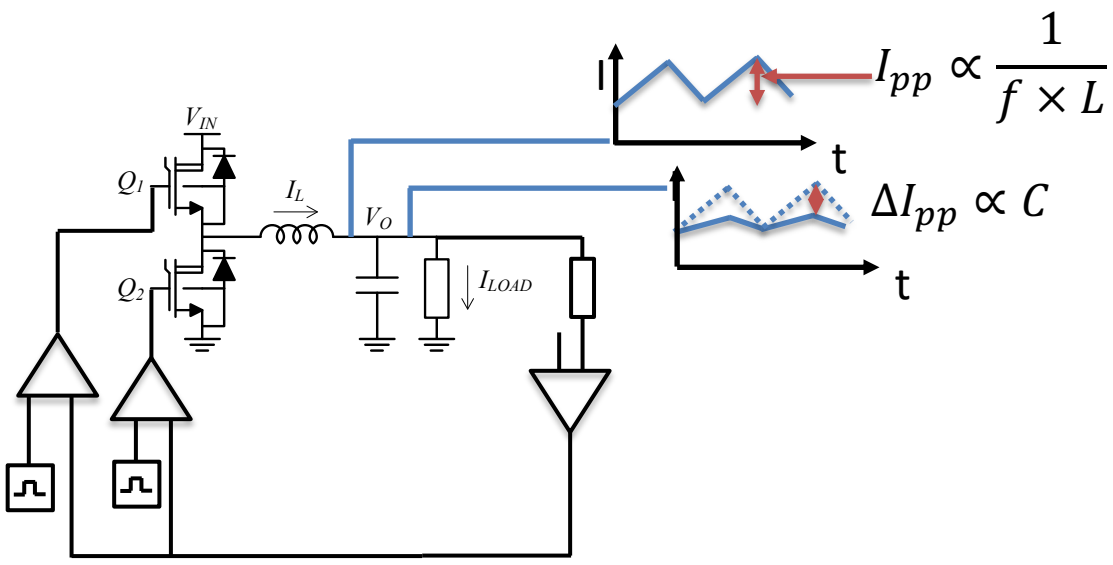


Figure 3. Schematic of a typical DC-DC buck converter using an inductor and capacitor, showing the effect of capacitance and inductance values on output ripple current

1.3 Capacitor Materials and Processes to Date: Science and Technology

To perform materials research on improving capacitor technology, it is important to understand from a materials perspective where capacitance is derived. The equation for capacitance is as follows:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{2}$$

where ε_0 is the permittivity of free space, ε_r is the permittivity of the dielectric material separating the two conducting electrode plates in the capacitor, relative to air, *A* is the mutual area of the electrode plates, and *d* is the distance between the electrodes, or the thickness of the dielectric material. The basic structure of the most basic type of capacitor, the parallel plate capacitor, is shown in Figure 4. The permittivity of the dielectric is a measure of its ability to block an electric field due to the polarization of the internal electronic, atomic and dipolar species. This is important for high capacitance density. At the same time, a thinner dielectric can provide higher capacitance, so the

ability to process one with nanoscale control over uniformity and thickness is critical. It must also have low levels of defects, so that leakage current between electrode plates is not too high. This is one of the limiting factors for how thin the dielectric can be made, before dielectric breakdown occurs.

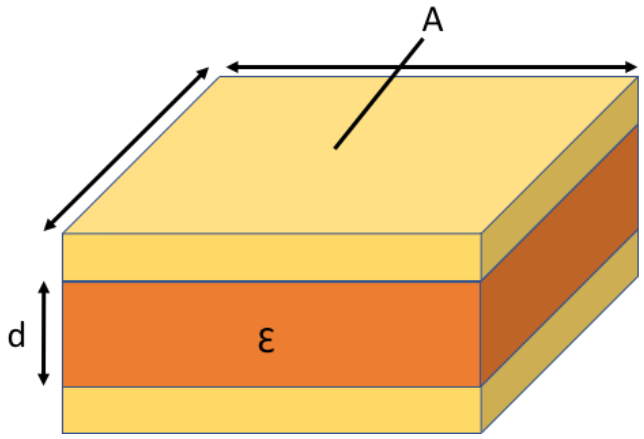


Figure 4. Schematic of a parallel plate capacitor comprised of two conducting electrodes separated by a dielectric material

In IVRs today, parallel plate capacitors, or metal-insulator-metal (MIM) capacitors are commonly used on-chip since they can be easily processed and implemented. A medium permittivity oxide, such as Al_2O_3, Ta_2O_5, HfO_2, or ZrO_2, can be vapor-deposited through atomic layer deposition (ALD), chemical vapor deposition (CVD), or even physically deposited. This dielectric is sandwiched between conductive layers of material, often aluminum, thus forming the capacitor layers. Though they are small, they are limited in capacitance density by their area and medium-permittivity dielectrics, and thus only serve as high-frequency decoupling capacitors.

On the other hand, input and energy-transfer capacitors must have larger capacitance values to keep the power efficiency of the IVR to a reasonable level. For these, multi-layer ceramic capacitors (MLCCs), with stacked layers of ferroelectrics and

metallic electrodes, are usually surface-mounted onto the package. Higher capacitance values can be achieved due to the ferroelectricity of the dielectric layers, providing orders of magnitude increase in permittivity. Often the material is a barium-titanate ($BaTiO_3$) derivative, which exhibit ferroelectric properties due to the transition of the perovskite structure to a tetragonal phase with reduced symmetry below the Curie Temperature (Figure 5). The tetragonal phase allows movement of the base-centered barium cation relative to the oxygen anions, which induces a polarization in the presence of an external electric field that is retained after removal of the field. However, the sensitivity of the crystal structure to temperature means that the power handling of these capacitors is limited, since higher power levels result in increased heating. Therefore, research focuses on ways to improve the stability of the ferroelectric crystal structure.

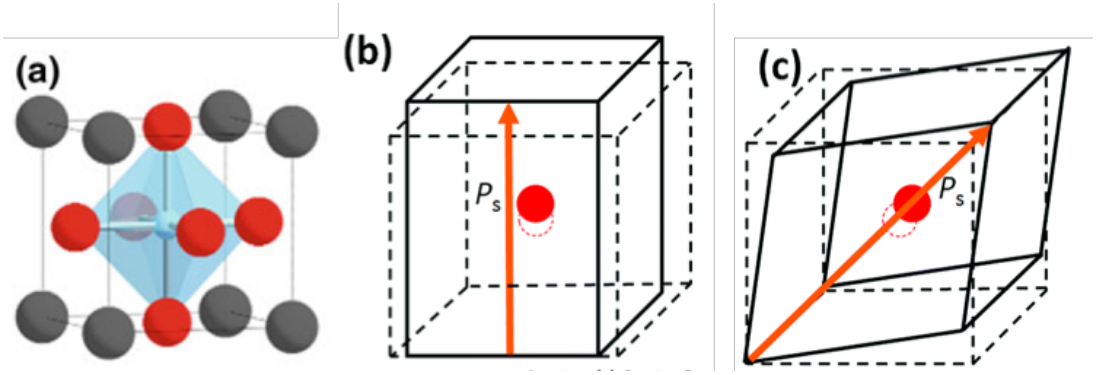


Figure 5. Perovskite structure of BaTiO3 in (a) cubic phase [18] (b) tetragonal phase (c) orthorhombic phase [19]. In the non-cubic phases, the ability for titanium movement within the unit cell gives rise to ferroelectricity

Alternatively, the surface area of the electrode can significantly affect the capacitance density of the device. Using high surface area structures for the electrodes, such as nanoparticles or nanowires, could significantly enhance performance of the capacitor even further. However, high-surface area structures can lead to other electrical design considerations that can limit capacitor performance, due to long conduction paths

that causes higher resistance and longer charge/discharge times. Therefore, it is important to consider the material structures for both the electrodes and dielectric materials.

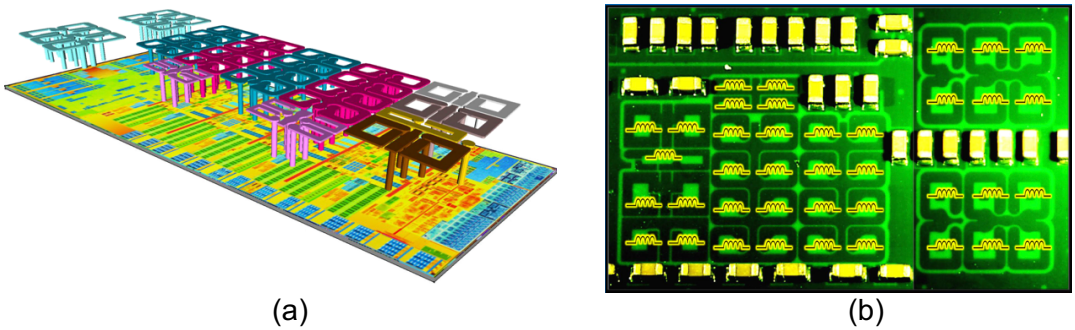
Current developmental work focuses on finding ways to improve component volumetric capacitance density while reducing the size and minimizing parasitic impedance, including the development of new, thinner, and more stable dielectric materials as well as surface area enhancement techniques for the electrode materials. The next section will discuss the capacitors seen in some examples of state-of-the-art IVRs.

1.4 Capacitors in State-of-the-Art IVRs

Today's voltage regulators primarily package the active components separately from the passive components, such as the capacitors and inductors. These components are then surface mounted on the board, relatively far from the microprocessing unit. However, advancements towards integrated voltage regulation are beginning to appear. On-chip, it is common to see the all of the active components, including the switches, drivers, and control, integrated together into a single power management integrated circuit (PMIC). This is especially common in low-to-medium power applications, where the switches do not have to be as large. However, this section will go further, and focus on voltage regulators that feature integrated passives as well, which generally occupy the largest volume in a PDN.

The fully integrated voltage regulator from Intel, or FIVR, is a huge step towards power conversion taking place fully on-package. The FIVR features inductors that sit directly beneath the PMIC in 3D. These inductors are essentially cooper windings that are surrounded by a non-magnetic epoxy-based molding compound, as shown in Figure

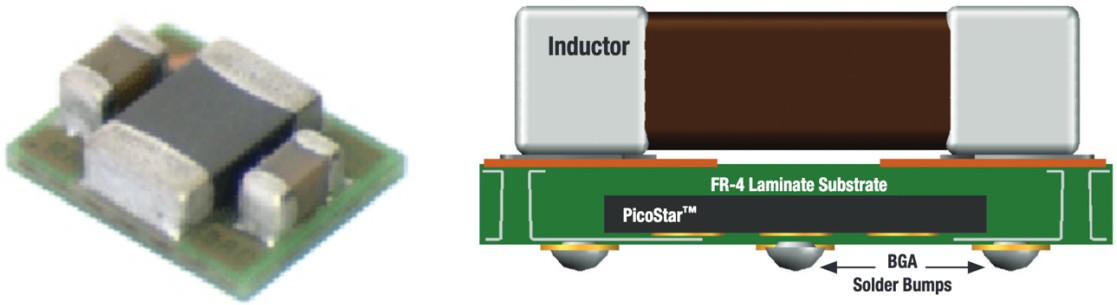
6. Since the epoxy material is non-magnetic, it has a low relative permeability μ_r close to that of air, or ~1. This mean that the inductance values that the inductors provide is quite low, on the order of 7 nH/A [20]. Additionally, the output capacitors are simply MIM capacitors, so the capacitance they provide is not very high (on the order of fF to pF). The input capacitors are surface-mounted multi-layer-ceramic capacitor (MLCCs) that use up package area. Since both the capacitance and inductance values are low, the IVR has to operate at very high switching frequencies of 140 MHz, so high that is begins to limit the efficiency of the system due to the switching losses. Also, the low capacitance and inductance values require the use of many phases and many components, using up a lot of area that could otherwise be used for other components, as shown in Figure 6. By improving the capacitance and inductance values of the passive components, as well as integrating all of them into thinner 3D structures, there could be an improvement in both power density and efficiency. Finally, the FIVR acts as only the last stage of power conversion, from ~1.7 V to ~1 V. There is still another power converter on board that converts from 12-20 V down to the ~1.7 V, so the high current rails must still run through the board and package. In a truly integrated solution, all of the conversion should be done on-package to limit this and save board space.



(a) (b)

Figure 6. (a) Epoxy-core inductor copper windings beneath PMIC (b) Top-view of surface-mounted MLCCs and inductor windings in Intel FIVR [21]

In another example, more of the power conversion is completed in a single step by using a ~5:1 V conversion. In this case, the PMIC itself is embedded in the substrate and the passive components are surface mounted on top Figure 7. Again, discrete MLCC solutions are used to provide the input and output decoupling capacitance. In this case, much of the volume of package is again used by capacitors and inductors, and the overall package is fairly thick, so that is must be placed on board rather than directly on the same package as the processor. Although this simplifies the PCB design, it still requires the system to run high current rails to and through the microprocessor package, and it does not provide a fully 3D IVR solution.



(a) (b)

Figure 7. Integrated voltage regulator featuring embedded PMIC and surface mounted passives in a single package solution (a) Top-view photograph and (b) diagram of cross-section [22]

From these examples, it is clear that there is a desire for more integrated solutions to power management in electronic systems. Packages with integrated actives and passives provide numerous benefits to system performance, but still face challenges before truly single-step, fully integrated voltage regulation can be achieved. These challenges are primarily related to the limitations of the passive components rather than the actives. For capacitors, surface-mounted MLCCs are the solution of choice since they have can provide decently large capacitance at higher switching frequency. However, the fact that they are surface mounted limits their integration capability, and

even then, there are material compatibility issues that limit their current or voltage ratings, thereby limiting the total power density of the module. Thus, there is a need for a new capacitor technology in IVRs that can provide ultra-high capacitance densities in ultra-small form factors while operating at high voltages, higher currents, and higher temperatures.

1.5 Capacitor Requirements in Power Conversion and Distribution

Emerging design requirements of power distribution networks in fully-integrated, single-stage, high power-density power conversion demand ultra-high capacitance densities to deliver up to 2 A/mm^2 with lower impedance of less than 10 mΩ by integrating them closer to the active components with lowest vertical distances. A set of requirements that significantly improve upon the current capacitor technologies can therefore be identified. The specific requirements for emerging capacitor technologies are defined and elaborated in this section.

The need for high capacitance density in IVRs is evident through the previous discussions. From Equation 1, the output ripple voltage is inversely proportional to the capacitance value of the output decoupling capacitor. Therefore, high-density capacitors can provide large capacitance values in smaller form factors, thereby ensuring a steady power output from the power converter. Equivalently, this means that higher power outputs can be achieved, since a certain level of output ripple is acceptable for a processing unit, and the amount of ripple will proportional to the total current being supplied. At the same time, we want to fit as much capacitance into as small of a volume as possible, since one of the ultimate goals of IVR is miniaturization and the capacitors take up such a large proportion of the volume in a typical voltage regulator today. Therefore, an ultra-high volumetric capacitance density is desired.

High frequency stability is also necessary to improve IVR power density. Also from Equation 1, a higher switching frequency is inversely proportional to the output ripple, so the best case would be to increase both the capacitance and switching frequency to maximize the possible power output in the system. A lower ESR helps to improve the decoupling capability of the capacitors. Additionally, the efficiency of the converter is equally important, so that minimal power is wasted and converted into heat. Therefore, minimizing the ESR of the capacitor is also critical.

To achieve fully integrated, ultra-small IVR, a capacitor with a small form factor that can be integrated in 3D is needed. Through such 3D integration, the need for decoupling capacitors is reduced. In addition, board and package area is not committed for decoupling capacitors. Also, the distance between the capacitor and switches is minimized, so that minimal conduction losses and parasitic inductance is created through the interconnects between them. Not only does this improve system efficiency and reduce heating, it also helps with the second objective of achieving higher frequency stability and reduced ESR.

Finally, even with all of these requirements in place, there will still be inherent heating in the converter due to the large current densities going through the conductors. Additionally, the embedding of the capacitors in close proximity to the active switches of the converter implies that the capacitors will see much higher temperatures than they otherwise would surface mounted onto a PCB. Thus, the capacitors must be able to withstand higher temperatures so that the can continue to operate even at maximum power output.

1.6 Research Objectives

The primary objective of this research is to develop and demonstrate high-density and integrated film capacitor technologies with unique nanostructures that can achieve the performance objectives in an ultra-small, thin-film format. The objectives are qualitatively described below, and then quantified along with the prior art, challenges and research tasks in Table 1:

1. High volumetric capacitance density of >1 $\mu F/mm^2$ at a thickness of 100 µm, or >10 $\mu F/mm^3$, so that large capacitance values can be achieved in ultra-small form factors
2. High frequency stability beyond 1 MHz and low equivalent series resistance (ESR) of <50 mΩ, so that the capacitor can operate at high switching frequencies with low losses
3. Ultra-thin form factor of 100 µm thickness with thin-film integration capability, so that the capacitor can be integrated in 3D by embedding directly within the IVR substrate
4. High temperature stability up to 125° C, so that the capacitor can handle high current levels while operating near the switches, and thus provide high power densities to the system

Table 1. Summary of research objectives, challenges, and tasks

Parameter		Objective	Prior Art	Challenges	Tasks
Capacitance Density at 1 MHz and 100 µm thickness	5 V	**>1 µF/mm^2**	<0.5 µF/mm^2	Balance need for high capacitance density with high frequency stability by optimizing electrode material nanostructure	**1. Capacitor design** using high-surface area, printed Ta nanoelectrode and electrochemically grown dielectric
	30-48 V	**50-100 nF/mm^2**	0.66 nF/mm^2		
Frequency Stability and ESR		**1-10 MHz ESR <50 milliohms**	• Ta: <300 kHz, >100 mΩ • MLCC: 100 MHz, 15-50 mΩ • Silicon: GHZ, 100 mΩ ESR		
3D Package Integration		• **100 µm interconnect** • **0% added area (3D integration)**	• Surface-mount devices • Low-density laminates or MIMs	Material compatibility with via formation and build-up processes	**2. Capacitor fabrication and integration** directly on silicon using scalable foil transfer and build up processes
Reliability at High Operating Temperature		**125 °C**	• High-ESR Ta Caps with MnO_2 cathode • Low-density paraelectric MLCCs • Silicon trench	Conducting polymers are susceptible to thermally induced moisture absorption and oxidation	**3. Capacitor Reliability:** Develop barrier-material strategy to limit moisture infiltration and evaluate capacitor reliability

In order to accomplish these objectives, an understanding of innovative electrode materials that can be formed into such nanostructures is needed. In addition, unique process innovations are required to realize such nanoelectrode structures on the wafer or in packages. Based on these research objectives, a carefully selected material system and capacitor structure is proposed.

1.6.1 Proposed Materials and Processes to Achieve Objectives

To meet the needs of high volumetric capacitance density, high-frequency stability and low ESR, and high temperature stability, a nanoporous tantalum-based capacitor thin-film is selected. A schematic of the proposed structure is shown in Figure 8. The use of a printed nanoparticle-based electrode structure provides an ultra-high

surface area-to-volume ratio for higher charge storage, while also achieving an ultra-thin form factor. Such a structure could be achieved by printing the tantalum nanoparticles as a slurry before sintering at high temperatures to form a continuous, high-surface area, metallic structure while removing impurities from the slurry.

Tantalum is chosen as the metal electrode material due to its low resistivity and ability to form a highly stable, high-permittivity dielectric of tantalum pentoxide (Ta_2O_5). In its amorphous form, Ta_2O_5 has as relative permittivity of ~22-25 that changes very little over a wide temperature range [23], although higher permittivity values have been reported depending on the film thickness and processing method [24-27]. Also, since the oxide can be electrochemically formed, the growth can be highly monitored and controlled down to nanoscale thicknesses with high uniformity. Finally, the absence of grain boundaries helps to limit conduction across the dielectric film, thereby minimizing dielectric losses of the capacitor [28].

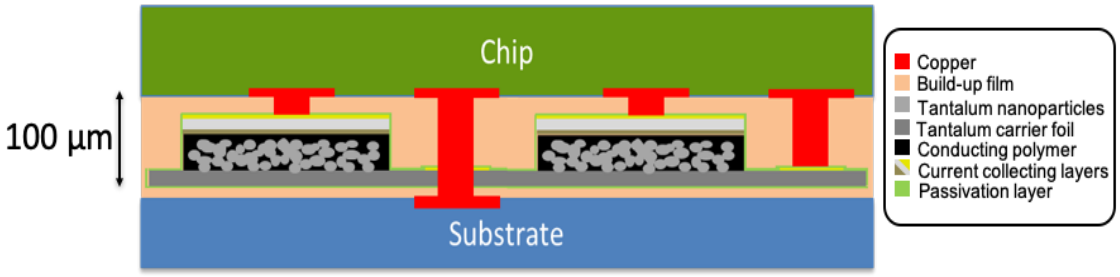


Figure 8. Proposed capacitor structure based on high-surface area, printed nanoporous films of tantalum

A conducting polymer suspension is chosen as the cathode material to infiltrate the nanoporous region and coat the metal-oxide nanoparticles with a low-resistivity material. Poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) is a highly conductive polymer mixture with capability of being deposited as a low-viscosity

aqueous suspension, so that it may fully enter and fill the nanoporous region of the capacitor [29-31]. Additionally, the PEDOT:PSS cathode material can provide the capacitor with self-healing capabilities. The mechanism for healing is theorized to be related to the local Joule heating at a defect site in the dielectric, as current shorts between electrodes. This heating creates a hot-spot, that can either evaporate the conducting polymer or induce the migration of oxygen ions into the PEDOT, thereby increasing its local resistivity at the defect site [32]. In the way, the defect site becomes effectively electrically isolated from the rest of the capacitor, and leakage current is reduced.

Finally, graphite and silver paste layers are used to create a low-resistance ohmic contact between the conducting polymer and the copper interconnects, connecting the capacitor to the rest of the PDN. The graphite layer is used to help prevent electromigration of silver ions to the internal capacitor structure by acting as a diffusion barrier. Otherwise, the silver ions could act as defect sites at the dielectric interface leading to Poole-Frenkel migration of charge across the dielectric [28]. These layers can also be printed. Combining the silver paste and graphite layers, conducting polymer cathode, Ta_2O_5 dielectric, and printed tantalum nanoparticle anode, an ultra-thin capacitor structure is formed.

1.7 Technical Challenges and Research Tasks

With the research motivation for capacitors in power delivery and distribution identified, objectives determined, and the proposed capacitor structure understood, the technical challenges related to achieving this must be considered. The first challenge is obtaining high capacitance density at ultra-small form factors while also maintaining high frequency stability. For high frequency stability and low ESR, the impedance of the

electrode structure must be kept as low as possible. This is especially difficult to do with high surface area structures, where thin, long conduction paths are used as the electrode structure which can result in higher resistance and parasitic inductance than what is desired. Therefore, the challenge is balancing the need for high capacitance density with the need for the ability to operate at high frequencies with low ESR. Thus, a model needs to be developed that can predict the relationship between capacitor nanostructure and bulk electrical properties, so that the structure can be optimized to achieve the best combination of capacitance density and frequency stability.

The second challenge stems from the need to fabricate the capacitor in a method that provides a thin final capacitor structure with the ability to be integrated in 3D directly beneath the IVR switches. This requirement for thin-film processing of such a complex capacitor structure with a breadth of materials and interfaces will take careful consideration of the material stability under various chemical environments, pressures, and temperatures that may be present in the fabrication and integration processes. Thus, the task becomes developing a fabrication process that maintains an ultra-thin, low loss structure without damaging the electrode and dielectric materials in the capacitor.

Finally, the last challenge is ensuring the capacitor is both stable and reliable at high operating temperatures. This is necessary to achieve both high current-handling and capability of operating as close as possible to the high-temperature active components, such as the power converter switches. The task is to understand all of the material degradation mechanisms associated with high-temperature environments, and then developing a method to limit these mechanisms. The research objectives, challenges, and tasks are summarized in Table 1.

CHAPTER 2: LITERATURE REVIEW

System performance and miniaturization with increased power densities has been continually driving innovations in on-chip component integration or embedding in the package. Embedded capacitor technology has been widely investigated for more than two decades but has been largely successful only as decoupling capacitors to suppress switching noise from high-frequency circuits due to the low capacitance values they provide. These capacitors are based on thin polymer, polymer composite or ceramic films with limited capacitance densities. Recent advancements have led to commercialization of some ferroelectric-based capacitor films, which can provide orders of magnitude improvements in capacitance density but are still limited to planar structures with low voltage and low temperature applications. Capacitors based on high-surface area silicon templates present an opportunity for high capacitance density and stability, with the benefit on-chip compatibility and employment of well-known silicon packaging techniques. Finally, valve-metal based capacitors, such as those based on aluminum and tantalum, can provide some of the highest capacitance and power densities, but current technical challenges keep embedded versions of these capacitors in the development stages. This chapter will review research efforts in each of these capacitor classes and what material advancements have enabled incremental improvements towards achieving one or all of the previously presented objectives of this research.

2.1 Organic and Composite Laminate Films

Organic laminates are currently the substrate of choice for most electronic packages, and this is primarily due to their low cost. Therefore, metalized organic films

provide a package-compatible capacitor technology that can be easily implemented into existing systems. Like the organic dielectrics used as a package material, the organics used as a capacitor dielectric material should have low losses, which includes conduction losses, losses from charge absorption and desorption, and polarization losses. However, unlike the dielectrics used as package materials, it is highly desirable for capacitor dielectrics to have a high permittivity value. Unfortunately, most polymers do not have a high density of strong polarization groups within their structure, thus limiting the maximum permittivity values that can be achieved.

Biaxially oriented polypropylene (BOPP) is one commonly-used polymer dielectric material due to its high stability and low losses. The polypropylene film is strained bi-axially as it is extruded, resulting in the orientation of the polymer chains in perpendicular directions. The resulting structure has greater chemical stability, higher permittivity, and higher dielectric breakdown strength than its unoriented counterpart [33]. One benefit of using this format of capacitor is the thin metallization that acts as the electrode material can provide self-healing capabilities to the capacitor. This occurs through resistive heating of the metallization at defect sites in the polymer dielectric leading to evaporation of the metal and polymer. However, one issue is that the material is only stable up to ~125° C before the capacitance begins to drop. While this is probably sufficient for most applications, more important is that the dielectric constant is still quite low (~2.2), limiting the capacitance densities that can be achieved using the material. Additionally, it is difficult to achieve a highly uniform sub-micron film. Other organic dielectrics exist, but face similar issues. Table 2 provides some of the critical material properties of other types of polymer dielectrics used in polymer film capacitors [34].

Table 2. Material properties of polymer dielectrics common in film capacitors [32]

Film material	PP	PET	PEN	PPS
Dielectric constant, ε_r	2.2	3.3	3	3
Dissipation factor (%@1kHz)	0.02	0.5	0.4	0.05
Insulation resistance (MΩ*μF)	> 100k	> 25k	> 25k	> 50k
Dielectric absorption (%)	0.01	0.5	0.8	0.05
Capacitance change (%) -40 ºC - +100 ºC	-3.5	+6	+5	-1
Typical best tolerance (±%)	1	5	5	1
Max operating temperature (ºC)	125	140	150	175
Stability/year (%)	0.2	1.0	1.0	0.3
Min. commercial thickness (μm)	2.5	0.9 (0.7)	1.4	1.2
Melting point (°C)	170	254	266	285

To improve the permittivity of laminate films, the addition of high-permittivity particles to the laminate matrix has been shown to result in a permittivity between those of the material constituents, analogous to the law of mixtures used to predict the mechanical properties of composite materials [35-41]. In an example, an embeddable laminate capacitor with copper thickness down to 6 μm is used to achieve up to 6.2 nF/cm^2 (Figure 9) [42]. The permittivity is achieved using $BaTiO_3$-based filler particles.

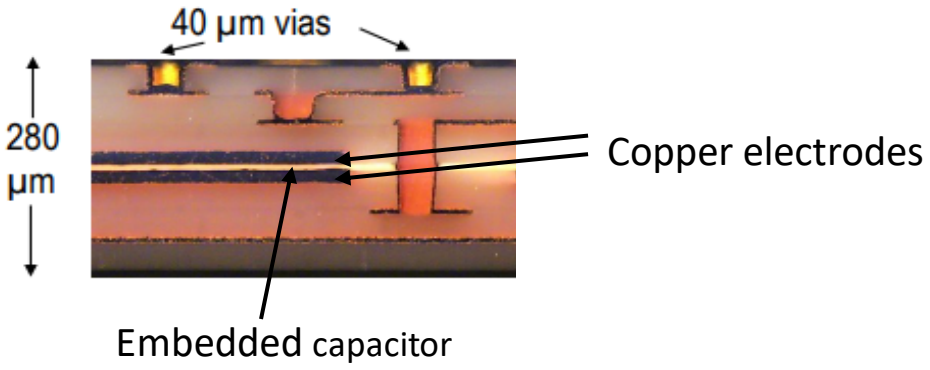
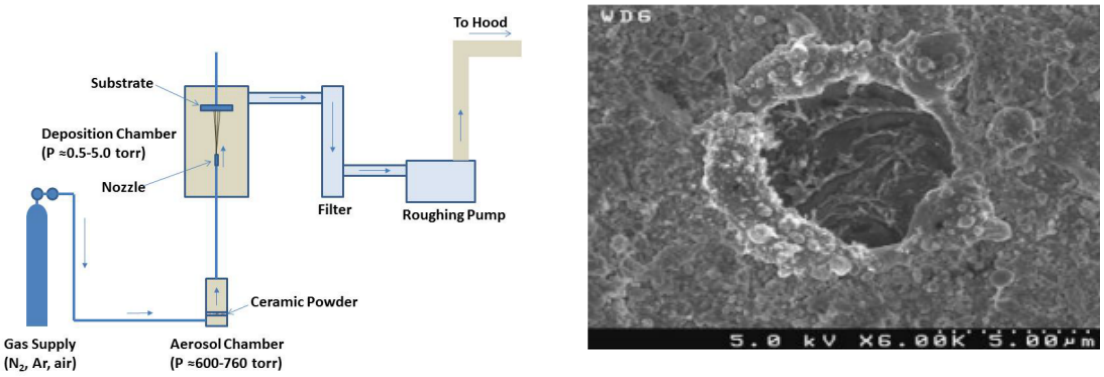


Figure 9. C-Ply high-permittivity laminate from 3M embedded in substrate [42]

To further improve the volumetric density of polymer films capacitors, Argonne National Lab in collaboration with Pennsylvania State University, ANL, Delphi, and Sigma is developing a composite dielectric based on a polyimide layer and a $Pb_{1-x}(La_x)ZrTiO_3$

(PLZT) layer [43]. The PLZT layer is deposited in a cost-effective approach using room-temperature aerosol deposition onto a metallized polyimide film before forming the final electrode and winding into a bulk capacitor (Figure 10). With the addition of the PLZT layer, the relative permittivity jumps from ~3 to ~80. In this way, the capacitor moves closer towards the volumetric density of ceramic capacitors while retaining the self-healing properties and reliability of polymer film capacitors. The capacitors demonstrated capability up to 150° C operation, but the high-frequency loss remains large.



(a) (b)

Figure 10. PLZT-Polyimide composite-dielectric capacitor with (a) aerosol deposited PLZT ceramic dielectric and (b) self-healing ability of the dielectric film due to evaporation of Al electrode at defect site [41]

Other research that have also focused on raising the power density have used purely polymer-based composite dielectrics. In a collaboration involving Polymer Plus, Oak-Ridge National Labs, and Case Western Reserve, co-extrusion of a high-permittivity material together with a high breakdown strength, low-loss material resulted in a synergistic combination of the two (Figure 11) [44]. The material achieves an improved dielectric constant of ~4 (compared to traditional polymer dielectrics), a dielectric strength of 1000 V/µm and operation up to 150° C. The film can be extruded using existing methods

to thicknesses from 3.5 μm to 15 μm. The dielectric loss and leakage currents are higher than conventional BOPP, so some developmental work is still needed.

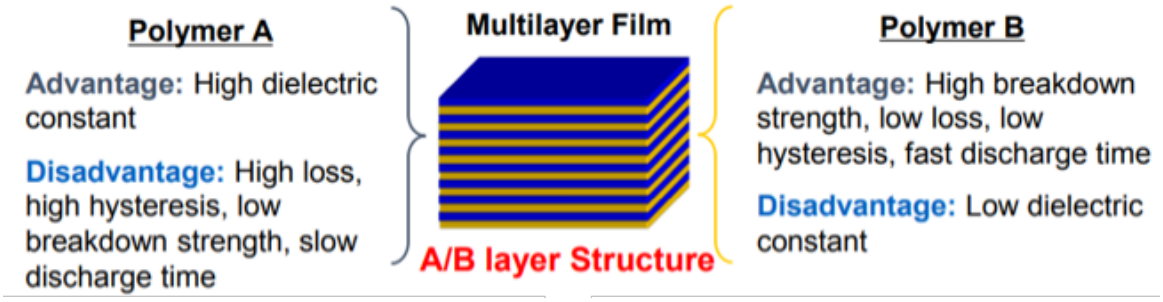


Figure 11. Enhancing performance of polymer film dielectric using multilayer structure [42]

While laminate composites do a good job of achieving low-impedance filtering and high stability, the capacitance is clearly still limited. As soon as the polymer matrix is added to the ceramic particles, the dielectric constant drops dramatically down to <30, limiting the use for energy storage applications. Various models exist to explain the observed reduction in permittivity, but they all are based largely on the volume fraction of the constituents as well the shape and continuity of the phases [35, 39-41]. One such model is the brick-layer model [41]:

$$\frac{1}{\varepsilon_{eff}} = \frac{v_1}{\varepsilon_1} + \frac{g v_2}{\varepsilon_2} \tag{3}$$

where ε_{eff} is the effective permittivity, ε_1 and ε_2 are the permittivity of phases 1 and 2, v_1 and v_2 are the volume fractions of phase 1 and 2, and g is a fitting parameter that depends on the geometry of the system. As can be seen, the effective permittivity is limited by the material constituent of lower permittivity, and only so much can be gained by adding ferroelectric fillers.

In another approach to improve the permittivity of the polymer itself, side-chain groups with high polarizability can be added to an organic-inorganic polymer chain using sol-gel processing to attain a dramatic increase in permittivity relative to conventional polymer dielectric films. Perry et al. demonstrated a dielectric constant of 20 from 1 kHz - 1 MHz and a loss of 0.01-0.1 in the same frequency range using this technique (Figure 12) [45]. The frequency stability and low loss of the dielectric can be seen in the thin hysteresis loop in the polarization curve. New polymer dielectrics like these enable more compact film capacitors with higher operating frequencies. Thus, much of the issues with polymer film capacitors are facing rapid improvements, including enhanced densities, improved frequency stability, and high temperature stability. Still, with a limited permittivity and a planar structure, the capacitance density will remain limited.

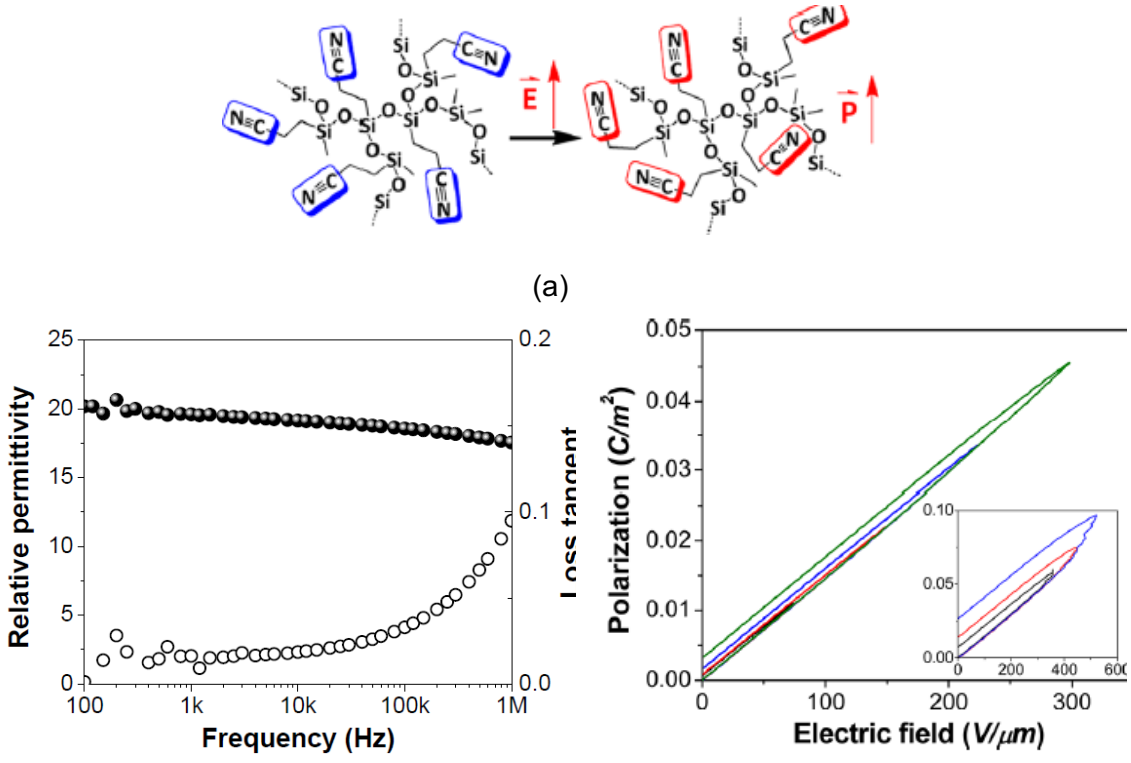


Figure 12. High permittivity sol-gel dielectric with (a) polarizable side-chain structure (b) high permittivity and low loss up to 1 MHz and (c) minimal polarization hysteresis [43]

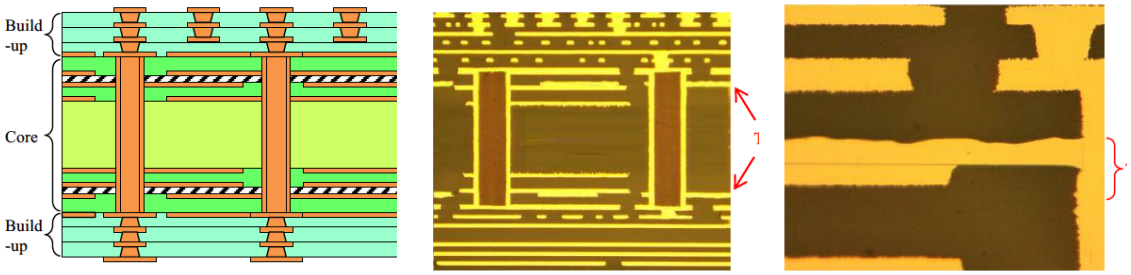
2.2 Embedded Ferroelectric Films

Ferroelectrics are a different class of materials that provide orders of magnitude increase in relative permittivity compared to other materials due to a dipole polarization mechanism in the atomic structure. An example of this is in the crystal structure of the ceramic barium titanate ($BaTiO_3$), which exhibits ferroelectric properties due to the transition of the perovskite structure to a tetragonal phase with reduced symmetry below the Curie Temperature (T_C). The tetragonal phase allows movement of the base-centered barium cation relative to the oxygen anions, which induces a polarization in the presence of an external electric field. Due to their ferroelectricity, relative permittivity values on the order of 10^3-10^5 can be obtained. For use in capacitors and other applications, changes to the material, often in the form of dopants, must be made to improve the temperature stability [46]. Even so, the relative permittivity is an order of magnitude or more above that of typical paraelectric materials, or materials that do not exhibit a spontaneous polarization and only become polarized upon the application of an electric field. This makes barium titanate (BTO) incredibly useful for high-volumetric density capacitors.

While integrated ferroelectric ceramics are an attractive option because of the low loss and high capacitance density they provide, ceramic capacitors require high-temperature processing due to the solid-state diffusion reaction between $BaCO_3$ and TiO_2 particles that takes place at 950 to 1200° C [47]. These firing temperatures are incompatible with the rest of the packages, and thus remain primarily discrete components formed separately. To form ceramic capacitors directly on-chip, lower processing temperatures are required. Much effort has been on using sol-gel processing to achieve this, but this still requires a final high-temperature annealing step. Additionally, development of the dielectric itself is ongoing, with efforts focusing on the addition of

dopants or reduction of grain-size to lower the firing temperature while maintaining high-permittivity and reliability. Alternatively, the thin-film ceramics can be formed separately on a carrier foil in a panel-scale approach, and later transferred to the package.

In an example of the foil-transfer approach, Tanaka et al. demonstrated a thin-film ceramic layer of $BaSrTiO_3$ (BST) in 2008 that was sandwiched between two electrodes and embedded in organic package [48]. With a film thickness of <1 μm and a high permittivity, an embedded capacitance of >1.5 $\mu F/cm^2$ was achieved. Since then, material advancements have allowed for further dielectric thinning. In one example, a 0.6 μm dielectric is sandwiched between two conductor layers, a nickel bottom electrode and a copper top electrode, which are both patterned to form the thin-film capacitor (TFC) layer. The TFC layer is then laminated onto a core substrate, where further RDL can take place. Akahoshi et al. has shown capability of producing an organic-core package with dual sided TFC layers using this technology (Figure 13) [49]. Using TFC layers instead of surface-mounted capacitors significantly reduced the power supply impedance up to ~300 MHz (Figure 14).



(a) (b) (c)

Figure 13. (a) Schematic and (b) cross-section of thin-film capacitors embedded in organic package. (c) Patterned electrodes connected to through-package via [47]

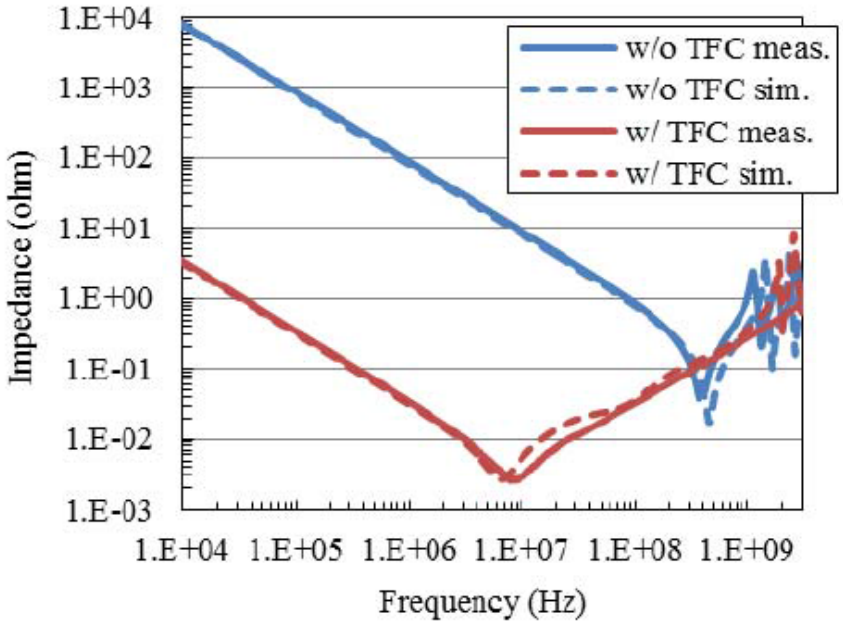


Figure 14. Reduced impedance due to TDK thin-film capacitors embedded in package [47]

To be able to achieve thinner ferroelectric films that remain reliable over the lifetime of the capacitor, it is critical to prevent the migration of oxygen vacancies. After firing in a reducing atmosphere, oxygen vacancies always remain in the dielectric. These positively charged vacancies migrate towards the negative cathode during operation and cause a locally increased electric field where they accumulate. This leads to premature breakdown and failure. Oxygen vacancy migration is considered to dominate the reliability of these dielectrics. Therefore, it is of great interest to minimize their electromigration so that higher-density ferroelectric capacitor films can be obtained without sacrificing component lifetime. There are three main ways in which oxygen vacancy electromigration can be reduced: controlling grain boundaries, controlling the grain interior, and control of the electrode interface [50]. To the first point, a high number of uniform grain boundaries, or equivalently small and uniform grains, helps improve reliability. During particle formation, a calcination process is used to form the $BaTiO_3$ particles. Longer calcination leads to

smaller grain size, but also adds impurities to the materials [47]. Therefore, the grain size is limited. To the second point, doping the material with certain species such as Ca^{2+}, Mn^{2+}, and Mg^{2+} can improve insulation resistance and limit oxygen vacancy mobility through the structure. Finally, to the third point, a homogenous electrode-dielectric interface is needed to keep the electric field uniform across the dielectric. These research efforts are summarized in Figure 15.

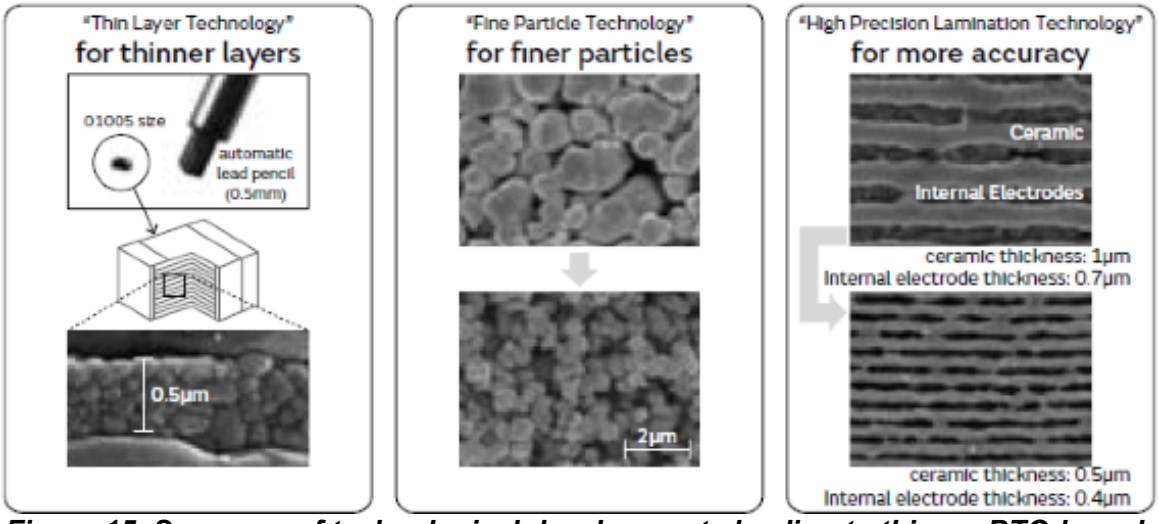


Figure 15. Summary of technological developments leading to thinner BTO-based dielectrics [50]

Even with these developments, there is still the issue of temperature stability that ferroelectrics are especially susceptible to. Due to their ferroelectric nature, higher temperatures reduce the chance of dipoles remaining in pace to counteract the capacitor's electric field. This leads to significant changes in the permittivity of the material with changes in temperature (Figure 16) [38, 39, 51, 52]. Thus, for high power densities where temperatures can increase dramatically during operation, paraelectric-based dielectrics are needed.

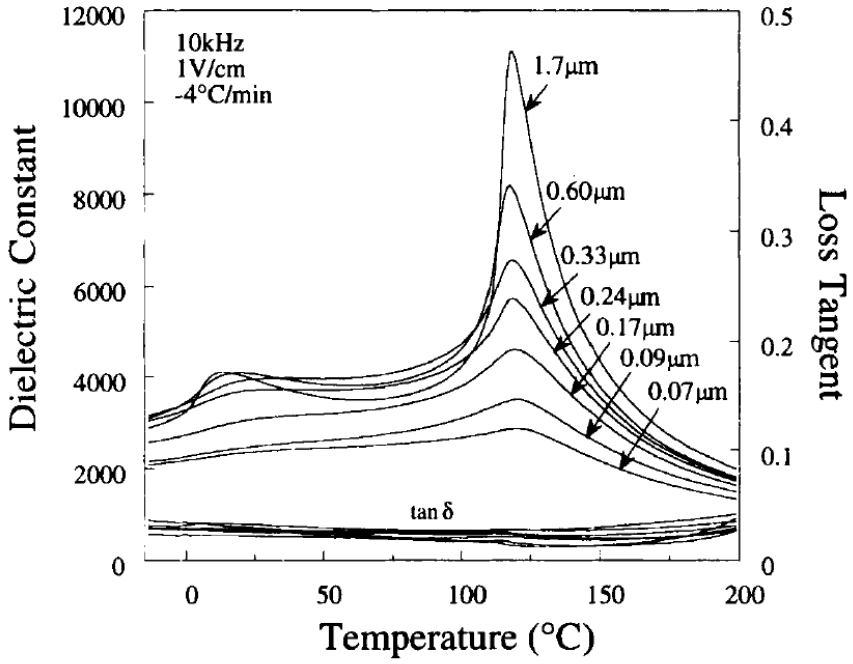


Figure 16. Effect of grain size on dielectric constant for BTO for small grain sizes [39]

2.3 Silicon Trench Capacitors

To provide an alternative to low capacitance density organic dielectric, and temperature-sensitive ferroelectrics, high surface area trench structures can be formed in silicon templates to achieve higher capacitance density while using a temperature-stable paraelectric material as the dielectric. Known as silicon trench capacitors, they are traditionally formed by using doped silicon as the base electrode material, thermally grown silicon oxide as the dielectric material, and then vapor-deposited doped silicon as the counter electrode as well. With a relative permittivity of only ~2.6 for silicon dioxide though, the density of these structures is still limited to ~25 nF/mm^2 [53]. Additionally, even highly doped silicon still has a high resistive compared to metals, so the ESR of these capacitors can still be quite high.

To improve silicon trench capacitor performance, other dielectrics and vapor-deposited electrodes have been explored. A list of possible high-permittivity oxides that

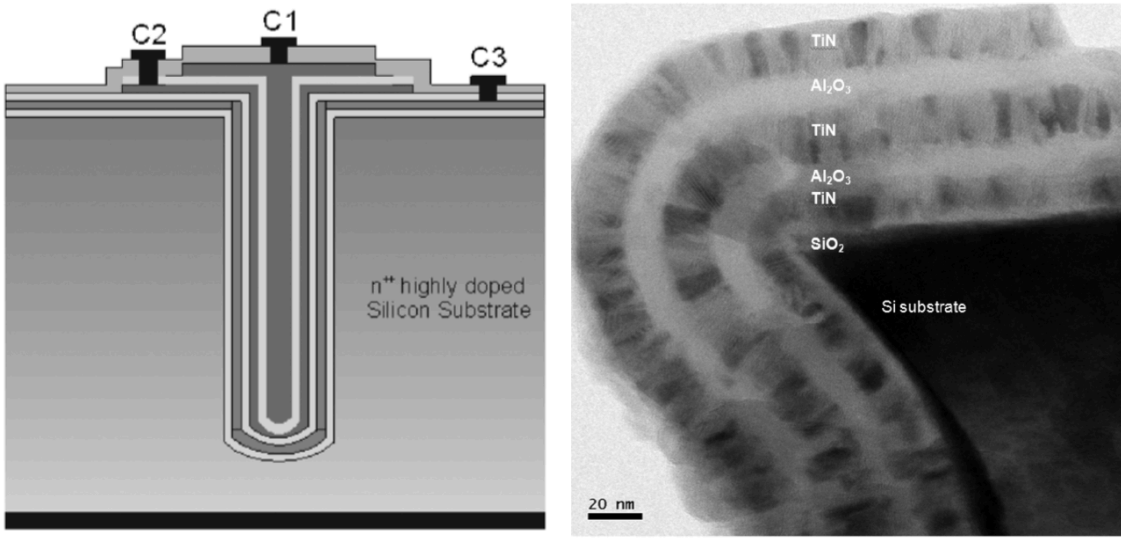
could serve as the dielectric material is included in Table 3 [54]. These oxide materials can be deposited by ALD, to achieve adequate step uniformity depending on the aspect ratio of the trench structures. A good dielectric should not only have a high dielectric constant, but also a large band offset on the electrode material so as to minimize conduction losses across the oxide. This band offset is dependent on the electrode work function relative to the dielectric.

Table 3. Dielectric constant (K), experimental band gap and (consensus) conduction band offset on Si various oxides [54]

	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8 (not ALD)
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8

It has been shown that the use of alumina (Al_2O_3) dielectrics with titanium nitride (TiN) electrodes can provide up to 500 nF/mm^2 capacitance density while keeping ESR down to ~10 mΩ, depending on the area used. Not only was the capacitance density enhanced with the use of a higher K dielectric, but also a triple metal-insulator-metal-

insulator-metal-insulator metal (MIMIMIM) structure was achieved by layering multiple deposition steps, so that within each trench were effectively three capacitors connected in parallel (Figure 17) [55]. Finally, tripod structures etched into silicon can provide even higher surface area than traditional trench structures, improving capacitance density even further [53]. Even with these enhancements, concerns over dielectric uniformity, processing costs, and band gap offsets leading to dielectric losses have led to continued research in the area.



(a) (b)

Figure 17. (a) Schematic of MIMIMIM trench capacitor (b) TEM image of TiN and Al_2O_3 layers at the bottom of the silicon trench capacitor [55]

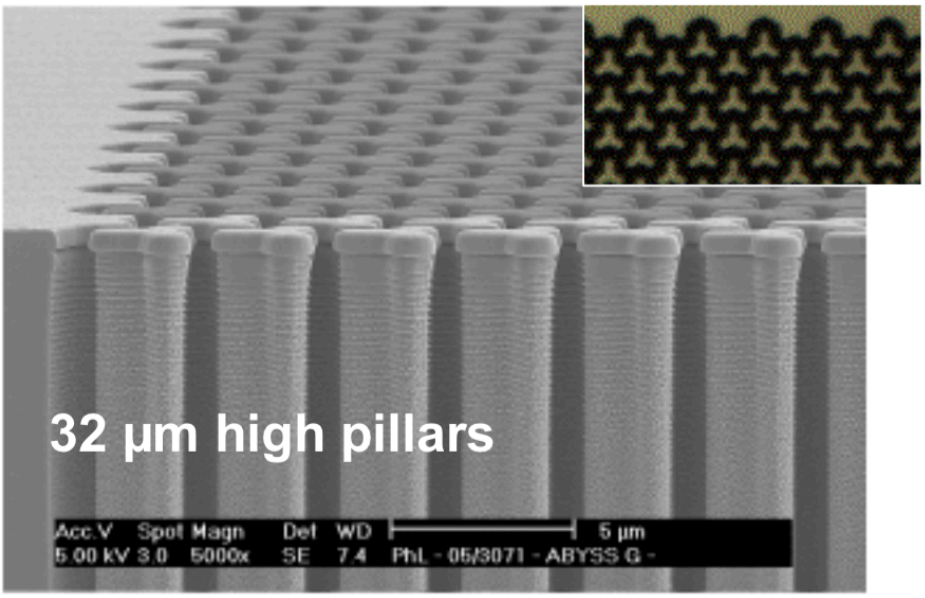
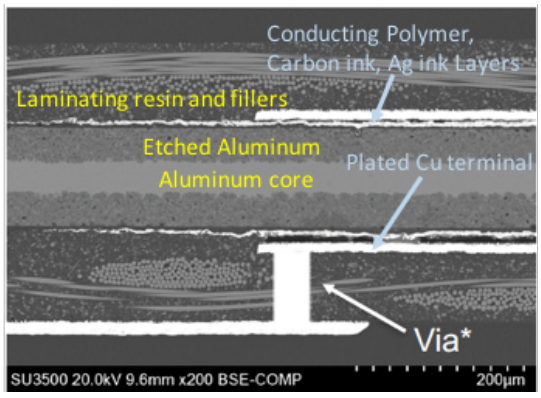


Figure 18. High surface area tripod structures etched into silicon [53]

2.4 Etched Aluminum Films

Rather than depositing alumina into silicon templates, it can be grown anodically directly on etched aluminum foils. These aluminum film capacitors can achieve similar capacitance densities or higher, due to the ability to use larger aspect ratios than what can be cost-effectively achieved with silicon trench structures. In one example, the aluminum sheet is formed, etched, and patterned on a copper foil so that integration of small footprints in a foil-transfer method are possible [56]. The high surface area comes from etching of the sheet, although vapor deposition is being explored as an additional means to increase the surface area even further. Conducting polymer cathode layers are deposited in controlled areas before final copper plating takes place to form a surface finish compatible with embedding. Finally, the capacitor sheet is applied to a transfer release film. In this way, the process is panel-scalable. While electrical measurements of the structure have not yet been provided, ambitious goals have been set for this project, including a capacitor thickness of only 50 µm while obtaining a capacitance density of 100

μm/cm^2. A partial cross-section of the embedded capacitor, as well as project design targets, is included in Figure 19.



(a)

Capability	Target
Rated voltage	2V-50V+
Capacitor size	≤1mm
Cap thickness	~50μm
Capacitance	≥100μF/cm^2
DC leakage	<50 nA/CV

(b)

Figure 19. Embedded aluminum polymer capacitor from KEMET (a) cross-section (b) design targets [54]

2.5 Nanoporous Tantalum Capacitors

Lastly, tantalum capacitors have potential to provide some of the highest volumetric densities due to the ultra-high surface areas and thin, high-permittivity dielectrics. At the same time, the Ta_2O_5 dielectric that can be anodically grown directly on the tantalum is temperature stable, enabling higher current densities and integration close to the IVR switches. However, the capacitors are generally formed as pressed nanoparticle pellets before sintering, which makes them bulky and incompatible with capacitor embedding. In fact, the thinnest tantalum chip capacitors available are >0.5 mm. Due to geometry constraints, there is a huge drop in density and volumetric efficiency as the thickness gets too low because of the size of casing relative to active electrode area. This problem is highlighted in Figure 20 [56].

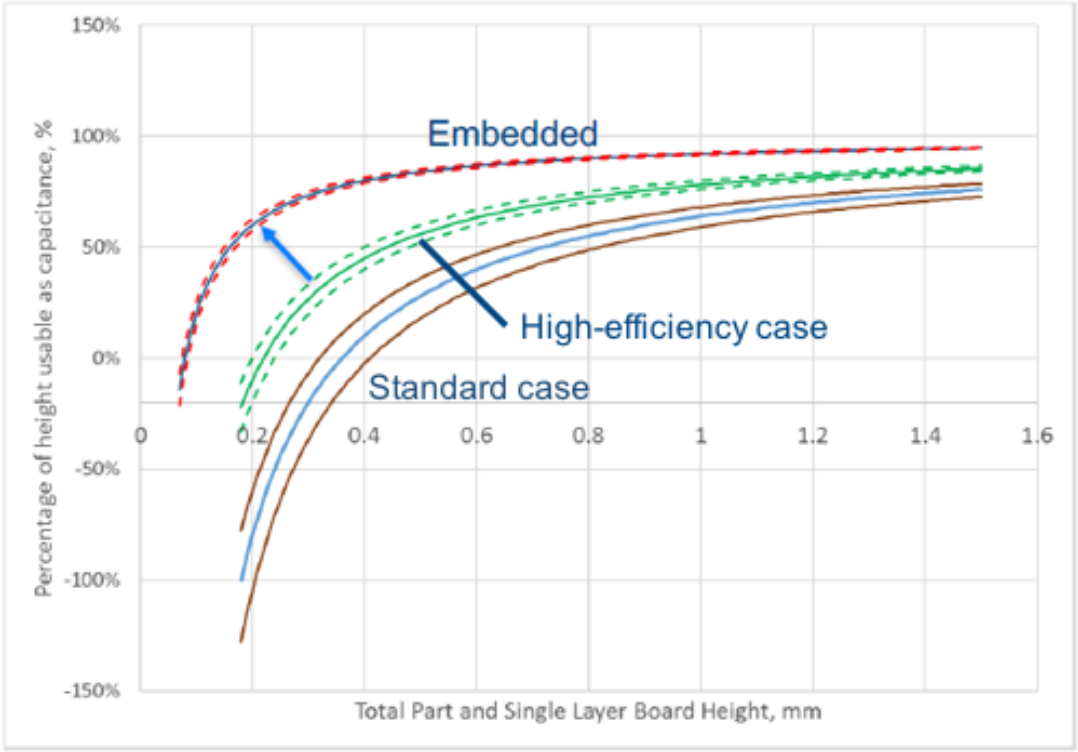


Figure 20. Dependence of volumetric efficiency on component height in electrolytic capacitors using standard designs versus new ultra-thin designs [56]

New tantalum-polymer chip capacitors with low profiles and improved volumetric efficiency due to improved packaging have become commercially available. Instead of standard termination, face-down constructions where the outer electrodes are connected to the inner pellet at the bottom of the case give some of the highest densities available for similar technologies (Figure 21). Despite the improvement, the thickness is still limited to > 0.5 mm, and usually much larger.

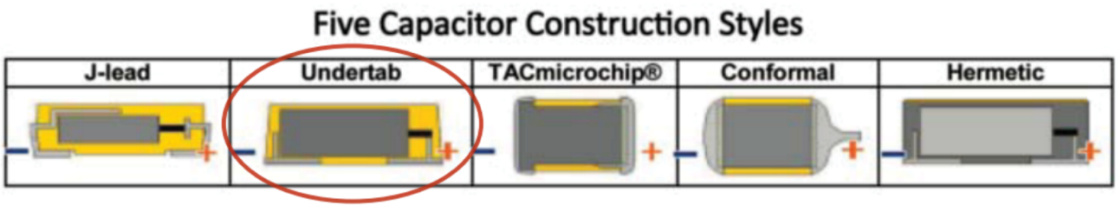


Figure 21. Tantalum-pellet capacitor packaging options. The face-down undertab construction gives the best combination of volumetric efficiency and impedance characteristics [57]

Although the embedded tantalum capacitors are still largely in developmental stages, they have the potential to provide some of the highest densities available compared to any other options from capacitors. This high density comes from the ultra-high surface area, tantalum nanoparticle-based anode, as well as the relatively high permittivity dielectric that can be formed down to nanometer-scale thicknesses in a controlled anodization process. Additionally, since the capacitors derive their high capacitance density from their high surface area rather than high-permittivity ferroelectric dielectrics, the capacitors can be integrated close to the active devices, where temperatures are generally much higher than for on-board components. While ferroelectrics are strongly sensitive to temperature fluctuations, paraelectric oxides like Al_2O_3 and Ta_2O_5 are not [51, 52]. Finally, with the use of a conducting polymer cathode material with self-healing properties, low leakage currents and high reliability components can be obtained. Continued development could see tantalum chip capacitor used in MHz-switching applications, paving the way for next-generation IVRs.

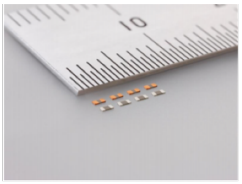
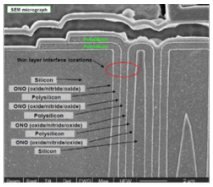
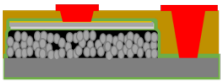
At the same time, the high surface area in tantalum capacitors results in long conduction path lengths for the charging and discharging current. The effect of this aspect of their structure on the electrical properties is higher equivalent series resistance (ESR) and poor frequency stability. While using conducting polymer instead of liquid electrolyte or MnO_2 helps improve the cathode conductivity, the capacitors are still limited to a maximum frequency of ~300 kHz or less. Thus, the capacitors are not currently compatible with IVR.

2.6 Summary of Prior Art

In summary, there are several different types of capacitor technologies with potential for use in package-integrated IVR modules. Polymer and composite laminates

have the advantage of thin structures, reliability, and ease of processing, but lack high capacitance density. Ferroelectric films can provide much higher capacitance densities, but are limited by their power handling. Silicon trench and etched aluminum-based capacitors can provide higher power densities, but are still limited in terms of capacitance density. Finally, there are tantalum capacitors, which do not exist in a format capable of embedding. Table 4 summarizes how these existing technologies compare to the capacitor proposed in this research.

Table 4. Summary of capacitor technology prior art and how it compares to proposed tantalum thin-film capacitors in this work

				
	Multi-layer Ferroelectric Films	**Silicon Trench**	**Ta-Polymer Chip**	**Ta Thin-film**
Volumetric Density	5 µF/mm^3	2 µF/mm^3	10 µF/mm^3	>20 µF/mm^3
Thickness	100 µm	100 µm	600 µm	100 µm
Freq. Stability	10-50 MHz	100 MHz-1 GHz	~300 kHz	>1 MHz
ESR	~10-50 mΩ	200 mΩ	500 mΩ	~50 mΩ
% ΔC/V	-13 % to -70% (1 to 4 V)	~ 0 %	~ 0 %	~ 0 %
Max. Temp	85° C	150° C	105° C	125° C

CHAPTER 3: CAPACITOR DESIGN

The objective of this chapter is to design a capacitor structure that can provide an ultra-high capacitance density of >1 μF/mm^2 at 100 μm thickness, while balancing the need to maintain high frequency stability and low losses. As previously mentioned, there is a need in next-generation computing for improved power delivery to meet the demanding processing speeds [2, 58]. Advanced power distribution and energy storage systems require high-density passive components that can operate at higher frequencies due to the increased power densities this can provide. To maintain stable power levels for increasingly power-hungry GPUs, CPUs, and ASICs, larger capacitance and inductance values are needed in smaller form factors while operating under faster switching speeds [5, 59]. Of those, capacitors have the potential to provide higher theoretical energy storage and power density compared to inductor-based power conversion systems [12, 15-17, 60]. Even in inductor-based power converters, large capacitance values can reduce the demand placed on inductive components.

Capacitors based on sintered nanoparticle-electrodes, such as tantalum capacitors, provide an ultra-high surface area-to-volume ratio, and thus the potential to provide some of the highest capacitance densities possible, since capacitance is directly related to electrode area [61]. Additionally, the porous nanostructure helps to delocalize heating and the dielectrics are generally thermally stable, such as is the case with Ta_2O_5, a paraelectric dielectric material used in tantalum capacitors. The combination of these two factors can enable higher current ratings compared to other types of capacitor technologies, thereby allowing for higher power densities [62, 63]. However, careful design of the electrode and dielectric structure is needed to manage the increased impedance that results from such a complex electrode system. If the impedance resulting from the

internal structure is not optimized, the capacitors cannot operate at the 1-100 MHz switching speeds desired in future-generation power converters [5, 64]. Large parasitic resistance results in reduced capacitance at higher frequencies when the RC time constant of the capacitor becomes too large compared to the period of the voltage transient, since there is not adequate time for charge and discharge of the capacitor [30, 65, 66]. Additionally, too much parasitic inductance will reduce the capacitor's transient performance and cause the capacitor to resonate beyond a certain frequency.

Thus, there is always a trade-off between the enhanced capacitance from using a nanoporous structure, such as those based on sintered nanoparticles, and the increased impedance the structure adds. Therefore, it is of great interest to understand the relationship between capacitor nanostructure and electrical performance so that is can be optimized for maximum performance. A model that can capture this relationship could then be used to quickly and accurately design capacitors to meet the needs of advanced power delivery systems. To date, no such model exists.

This chapter aims to provide a model-based approach to describe the material-property relationship in capacitor devices based on nanoparticle technology. Through characterization of real nanoparticle-based systems, the model is validated, and shown to provide an accurate prediction of the capacitor's electrical performance, including the equivalent series resistance (ESR) and capacitance. The accuracy of the model is achieved through the use of finite-element analysis (FEA) in conjunction with equivalent circuit construction. Thus, through the optimization of nanostructure, the model is used to calculate the theoretical limits of device performance, including capacitance density, ESR, and frequency stability.

3.1 Methods

3.1.1 Capacitance Model

To build the model, the geometry can first be broken up into individual RC units consisting of a single sintered nanoparticle. Each nanoparticle can be approximated as a sphere consisting of a conductive core (with radius R_{core}, conductivity σ_{core}, and permeability μ_{core}), an insulating dielectric shell (with thickness $t_{dielectric}$ and permittivity $\varepsilon_{dielectric}$), and an outer layer of some different conductive material (with thickness t_{outer} and conductivity σ_{outer}). The core and outer layer form the electrodes of the capacitor. The unit-cell geometry is then altered to account for sintering, which is needed to electrically connect the nanostructure. This is done by applying conservation of mass and approximating the neck regions between sintered particles as cylinders. To form the neck regions, there must be a relocation of mass from the spheres themselves. Therefore, for each cylinder neck, the volume V_{neck} is set to the equivalent of twice the volume V_{cap} of a hemispherical cap of height $k_{sint} \times R_{core}$ (Equation 4), where k_{sint} is a value <1. Additionally, the radius of each cylinder R_{neck} is set to the radius of the spherical caps R_{cap} that were used to form the new neck region (Equation 5). The constraints used in calculations are as follows: 12345678910111213

$$2 \times V_{cap} = \frac{1}{3}\pi(k_{sint}R_{core})^2 R_{core}(3 - k_{sint}) = \quad V_{neck} = \pi(2k_{sint}{R_{core}}^2 - (k_{sint}R_{core})^2) \tag{4}$$

$$R_{neck} = R_{cap} = \sqrt{2 \times k_{sint}R_{core}^2 - (k_{sint}R_{core})^2} \tag{5}$$

In this way, k_{sint} can be used to define the degree of sintering in the system, where larger values indicate increased sintering. As in a real particulate system, sintering is a diffusion-based process driven by the reduction in surface area, that proceeds through the thickening of neck regions and a densification, or reduction in distance between the particle centers. The approximated particle geometry before and after sintering is depicted in Figure 22a. Under these two constraints, the total length L_{np} and surface area S_{np} of each sintered nanoparticle can also be calculated:

$$L_{np} = (1 - k_{sint})2R_{core} + {V_{neck}}/{\pi R_{neck}^2} \quad (6)$$

$$S_{np} = 4\pi R_{core}^2 - 2\pi\left(R_{neck}^2 + (k_{sint}R_{core})^2\right) + (2\pi R_{neck}) \times {V_{neck}}/{\pi R_{neck}^2} \quad (7)$$

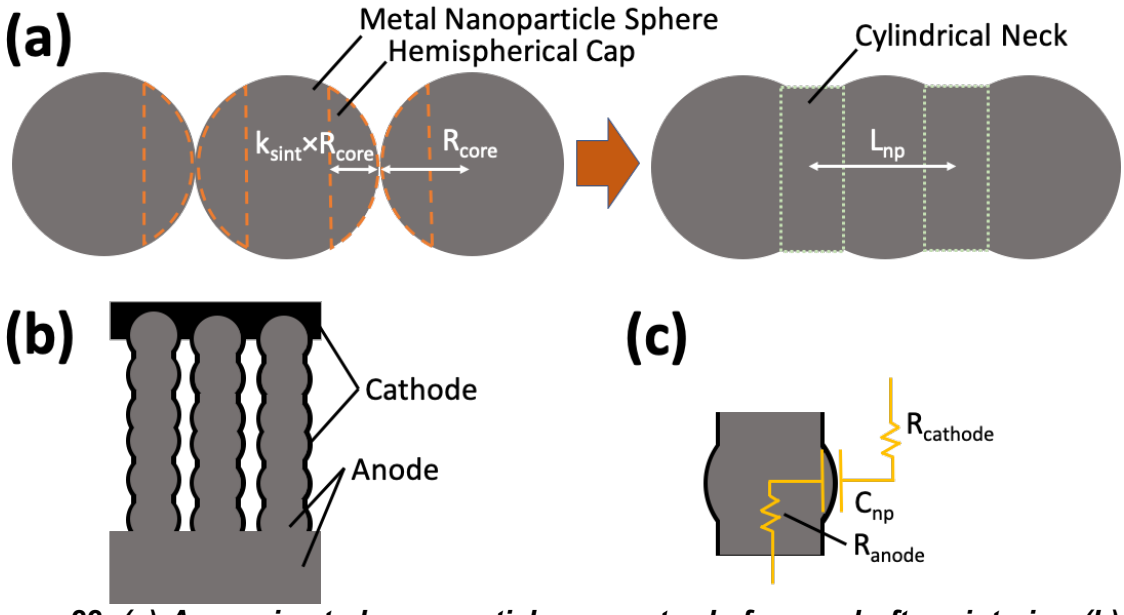


Figure 22. (a) Approximated nanoparticle geometry before and after sintering (b) Branches of nanoparticles (anode) coated in conductive material (c) Equivalent circuit for basic unit of capacitor structure: a sintered nanoparticle coated in oxide and conducting polymer shells

While the surface area is important for calculating the capacitance of the system, the length of each particle is also important for determination of the total number of nanoparticles in an arbitrary capacitor volume. The nanostructure can be thought of as many parallel branches that consist of a series of sintered nanoparticles, as shown in Figure 22b. To determine the volume density of nanoparticles and construct an appropriate equivalent circuit based on the nanostructure, it is important to understand both the number of nanoparticles, or RC elements, in a single branch as well as the area density of branches. Each nanoparticle has a resistance and capacitance associated with it, so each is considered an individual RC element represented by the equivalent circuit shown in Figure 22c. If one assumes the branch is a perfectly straight series of connected nanoparticles, then the total number of RC elements is simply the height of the nanoporous region H, or distance between the anode or cathode current collecting layers, divided by L_{np}. However, the nanostructure structure also has porosity, resulting in winding branches that are significantly longer than perfectly straight branches. Thus, a parameter k_{snake} is used to account for porosity. The number of nanoparticles N in a branch is then calculated:

$$N = k_{snake}\frac{H}{L_{np}} \tag{8}$$

After N is rounded to the nearest integer, the area density of branches must be calculated. If the sintered density of the nanoparticles ρ_{sint} is known, as is the density of the solid material of which the nanoparticles are made of, ρ_{solid}, then the packing density P_{pack} is just the ratio of the two. To then calculate the area density of branches, a face-centered-cubic (FCC) packing is used as an ideal model system, since this is the densest possible configuration of spherical particles with a volume packing density P_{FCC} of ~0.71.

The base unit cell can be thought to contain four vertical branches of spheres repeating periodically, and the area of the base unit cell is also known. Thus, the area density of branches P_{branch} is calculated with the following equation:

$$P_{branch} = \frac{4}{8(R_{core}^2 + t_{dielectric})} \frac{P_{pack}}{P_{FCC}} \frac{1}{k_{snake}} \tag{9}$$

where $t_{dielectric}$ is the thickness of the dielectric shell surrounding the particles, which must be accounted for when calculating the packing density. Again, the k_{snake} factor is used to account for the porosity of the system, since the branches are not perfectly straight. Since the number of nanoparticles in a single branch is increased by a factor of k_{snake}, then the number of branches must be decreased by the same factor to maintain the same overall packing density. With the sintered nanoparticle surface area S_{np} and number of nanoparticles per branch N known, the low-frequency branch capacitance C_{branch} can easily be calculated:

$$C_{branch} = N\varepsilon_{dielectric} {}^{S_{np}}/_{t_{dielectric}} \tag{10}$$

where $\varepsilon_{dielectric}$ is the dielectric permittivity. With C_{branch} and P_{branch} known, the overall capacitance density is simply the product of the two.

While the low-frequency capacitance density has been calculated, the high-frequency capacitance will be much lower due to the RC time constant of the capacitor elements being larger than the period of AC voltage excitation. At small excitation periods (or at high frequencies), the capacitor elements will not be able to fully contribute to the capacitance since they cannot fully charge and discharge. Thus, the capacitor's equivalent circuit must be considered. Other than the nanoparticles that form the branches of the

capacitor, current must also travel through the current collecting layers at the capacitor terminals. Additionally, there is always some contact resistance between layers as well as between the terminal and the measurement device. All of this can be accounted for in the equivalent circuit by considering additional series resistances. The complete equivalent circuit model to describe the structure-dependent impedance of the capacitor, without considering inductance, is shown in Figure 23. The number of RC elements on each branch is set to be *N*, while the total number of branches is just the product of branch area density and the total lateral area of the capacitor, $P_{branch} \times A_{lateral}$.

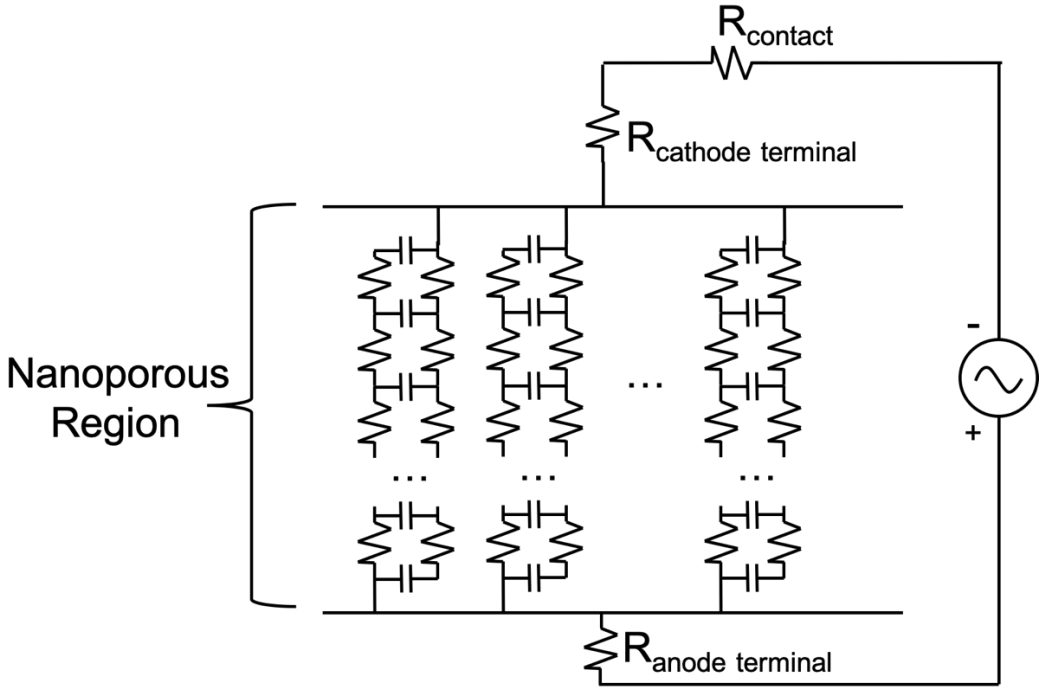


Figure 23. Equivalent RC ladder circuit of complete capacitor structure, with branches of sintered nanoparticles forming the RC ladder network within the nanoporous region of the capacitor

Based on the capacitor's equivalent circuit, the RC constant of each nanoparticle can be calculated. To accurately predict the RC constant of each element, a circuit analysis should be performed under the constraints that each capacitor element within the

branch should have the same voltage across it minus the voltage drop across the resistors between them. Since the initial charging current will be high, the voltage drop across resistors will also be high, and the capacitors can proceed with very different voltages across them. As charging proceeds, the current begins to drop, as does the voltage drop between capacitors. At the limit of long charging times, the charging current goes to zero and the capacitors maintain the same voltage across them, thus meaning the capacitors must charge together. Therefore, the capacitor charging cannot be modeled using a single exponent term, as in the case with a single capacitor. As the number of capacitor elements are increased, this calculation becomes increasingly complex to the point where it cannot feasibly be solved without the use of circuit simulation software. However, there are first-order approximations that can be used to provide bounds for prediction of the RC constant, and thus the frequency response of the full capacitor.

In the first method, Elmore's delay is used to approximate the RC constant τ_{Elmore} of each capacitor element. Elmore's delay is a first order approximation developed to predict the delay through and RC network, and is accurate for those capacitor elements with the largest RC constants [67]. However, this method begins to significantly underestimate the time delay for the capacitor elements with smaller RC constants, especially for longer charging times. Therefore, another method to approximate the RC constants of each capacitor element is needed.

In the second method, the capacitance used to calculate the RC constant is the branch capacitance C_{branch}, which is the sum of all the capacitance from each nanoparticle along the branch, while the series resistance value R_{series} will depend on the nanoparticle's position within the branch structure. For example, those nanoparticle elements closest to the anode terminal will have a much longer conduction path through the cathode material than through the anode material. The sum of the series resistances in the anode and cathode, as well as the contact resistance and resistance of the terminals, will form the

total resistance R_{series} for a given capacitor element. Therefore, the RC constant of each capacitor element $\tau_{Cbranch}$ is considered the product of the branch capacitance and its unique series resistance:

$$\tau_{Cbranch} = R_{series} \times C_{branch} \tag{11}$$

For those capacitor elements in the structure with the highest RC values, this method over predicts the RC time constant. However, it is found to be quite accurate for those elements with smaller RC constants.

Since the Elmore's delay model is accurate for the elements with the largest RC constants, and the branch capacitance method is accurate for those elements with smaller RC constants, the two models can be used together to predict the frequency stability of the overall capacitor. To verify this, a circuit simulation is performed on Simplis software using only ten capacitor elements in an RC ladder structure with arbitrary values (Figure 24a). Based on the rate at which the capacitors charge in the simulation, a best-fit line can be used to extract the effective RC constant τ of each capacitor element. These RC constants are obtained using best-fit lines of the following equation to simulation data comparing capacitor voltage versus charging time:

$$V = V_0(1 - e^{-t/\tau}) \tag{12}$$

where V is the voltage across the capacitor at any given time, and V_0 is the voltage once fully charged. A different τ is obtained by fitting data up to both ~63% and ~86.5% charged capacitors, since a single exponential term does not perfectly describe the capacitor

charging characteristics. The R^2 values obtained from the best fit lines are > 0.86 in all cases, and > 0.95 in all but two cases.

They are then compared to those predicted by Elmore's delay and the branch capacitance method (Figure 24b). As shown, the Elmore's delay method is accurate for predicting the maximum RC constant of the capacitor elements but underestimates the RC constant for other elements. The branch capacitance method is quite accurate up until the predicted RC constants become larger than the maximum predicted by Elmore's delay. Therefore, a hybrid method is proposed that combines the two methods, and is compared to circuit simulation results in Figure 24c. The RC constants in the hybrid method τ_{RC} are calculated using the following constraints:

$$\tau_{RC} = \tau_{Cbranch} \qquad \text{for } \tau_{Cbranch} < Max(\tau_{Elmore}) \tag{13}$$

$$\tau_{RC} = Max(\tau_{Elmore}) \qquad \text{for } \tau_{Cbranch} \geq Max(\tau_{Elmore}) \tag{14}$$

Figure 24 suggests that the hybrid method can provide the most accurate prediction of the frequency response of capacitance for each capacitor element, and thus the bulk capacitor.

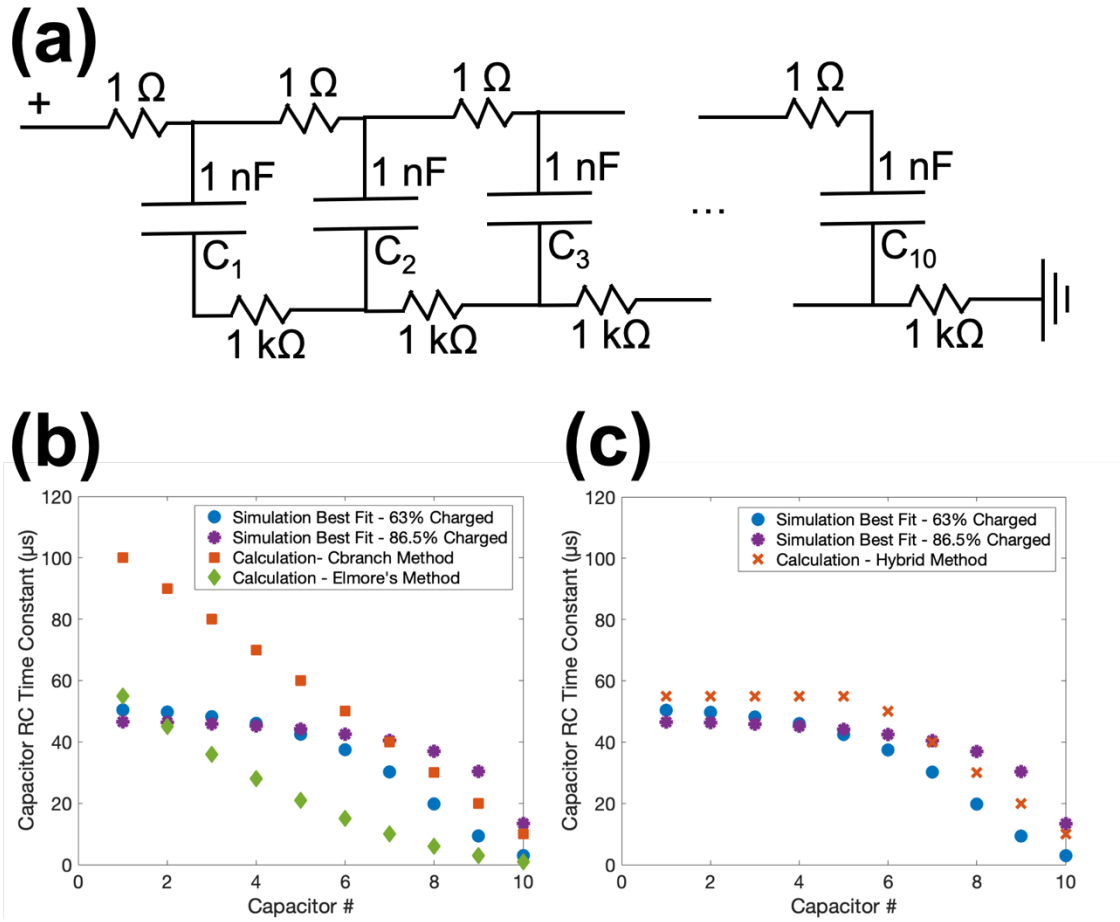


Figure 24. (a) RC ladder circuit used in DC circuit simulation to evaluate capacitor charging characteristics, with a total of ten capacitor elements and tweny resistor elements (b) Comparison of the best-fit RC constants for each capacitor element predicted from simulation software to the RC constants calculated using Elmore's delay and branch capacitance methods (c) Comparison of the best-fit RC constants to the RC constants calculated using the hybrid method

So far, only DC resistance has been considered. However, high frequency AC signal will result in internal eddy currents within a conductor that effectively reduce the cross-sectional area of the conductor and increase the resistance. The skin depth will be greater than the nanoparticle radius or outer layer thickness until >THz frequencies based on the equation used to calculate skin depth δ_s of a conductor:

$$\delta_s = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{15}$$

where f is the frequency of signal, μ is the conductor permeability, and σ is the conductor conductivity. Therefore, it is not necessary to consider AC resistance for the internal capacitor nanostructure. However, the terminals of the capacitor will have dimensions on the order of μm to mm, depending on the capacitor size, so the AC resistance must be considered in this case. In this model, the terminals are considered rectangles of the specified dimensions. After the skin depth is calculated, the series resistance of the termination layers $R_{terminal}$ is calculated using the resistivity of the material $\rho_{terminal}$, thickness of the material $t_{terminal}$, and cross-sectional area $A_{terminal}$ after accounting for skin depth with the following equation:

$$R_{terminal} = \frac{\rho_{terminal} t_{terminal}}{A_{terminal}} \tag{16}$$

Once the RC constants are calculated for a given frequency, each capacitor element contributes to the overall capacitance based on the amount it can charge and discharge during the period of the voltage transient associated with that operating frequency. The capacitance contribution from each element is calculated based on the following equation:

$$C_{np}^{i} = \varepsilon_{dielectric} \left({}^{S_{np}}/_{t_{dielectric}} \right) \left(1 - e^{-1/2 f \tau_{RC}} \right) \tag{17}$$

so that for low frequencies, the nanoparticle capacitance is at a maximum, but for higher frequencies, the effective capacitance contribution from that specific nanoparticle begins

to decrease depending on the RC constant of the element. A factor of 2 is used in the denominator of the exponential term since the capacitor must both charge and discharge over the period of the voltage transient. Again, the RC time constant is dominated by the series resistance R_{series}, which is unique to where the nanoparticle is within the nanoporous region of the capacitor. Then, if the total lateral area of the capacitor $A_{lateral}$ is known, the total effective capacitance at a given frequency C_f can be calculated:

$$C_f = A_{lateral} P_{branch} \sum_{1}^{N} C_{np}^{i} \tag{18}$$

where again, N is the number of nanoparticles within each branch.

3.1.2 ESR Model

For calculation of ESR, the same equivalent circuit shown in Figure 23 is used. First, the branch resistance R_{branch} is calculated by adding together all the cathode ($R_{cathode}$) and anode (R_{anode}) elements making up each nanoparticle along the branch. Unlike with the capacitor elements, the resistance values cannot easily be predicted, so an FEA simulation is used to extract these values. Ansys Maxwell software is used, and the resistance values are obtained using DC Conduction simulations based on the sintered nanoparticle geometry and the resistivity of the electrode materials. Based on the equivalent circuit, the branch resistances act in parallel while the termination resistance and contact resistance act in series. Again, the AC resistance of the termination layers must be considered. Thus, the ESR contribution from conduction, ESR_{σ}, is calculated as follows:

$$ESR_{\sigma} = \left(\frac{A_{lateral}P_{branch}}{R_{branch}}\right)^{-1} + R_{anode\ terminal} + R_{cathode\ termial} + R_{contact} \quad (19)$$

However, there are dielectric losses within the capacitor that also contribute to the total ESR, especially at low frequencies. These arise from a combination of dipole losses, dielectric conduction, and other undesired capacitor effects. The contribution to ESR from dielectric losses can be calculated using Equation 20:

$$ESR_{DF} = \frac{D_F}{2\pi f C} \quad (20)$$

where D_F is the dissipation factor, usually on the order of 10^{-2} for most dielectrics, and C is the total capacitance.

Finally, the total ESR is just the sum of the contributions from dielectric loss and conduction loss:

$$ESR = ESR_{\sigma} + ESR_{DF} \quad (21)$$

In summary, the model is developed by first defining the nanoparticle and device geometry. The resistance of the nanoparticle and conductive nanoparticle coating are then calculated from FEA calculations, and the capacitance contribution from each nanoparticle can be calculated based on geometry and dielectric material. These capacitance and resistance values are populated into a matrix whose size depends on the nanoparticle and device geometry. Finally, the frequency-dependent ESR and capacitance can be calculated from this matrix. The modeling process is summarized in Figure 25.

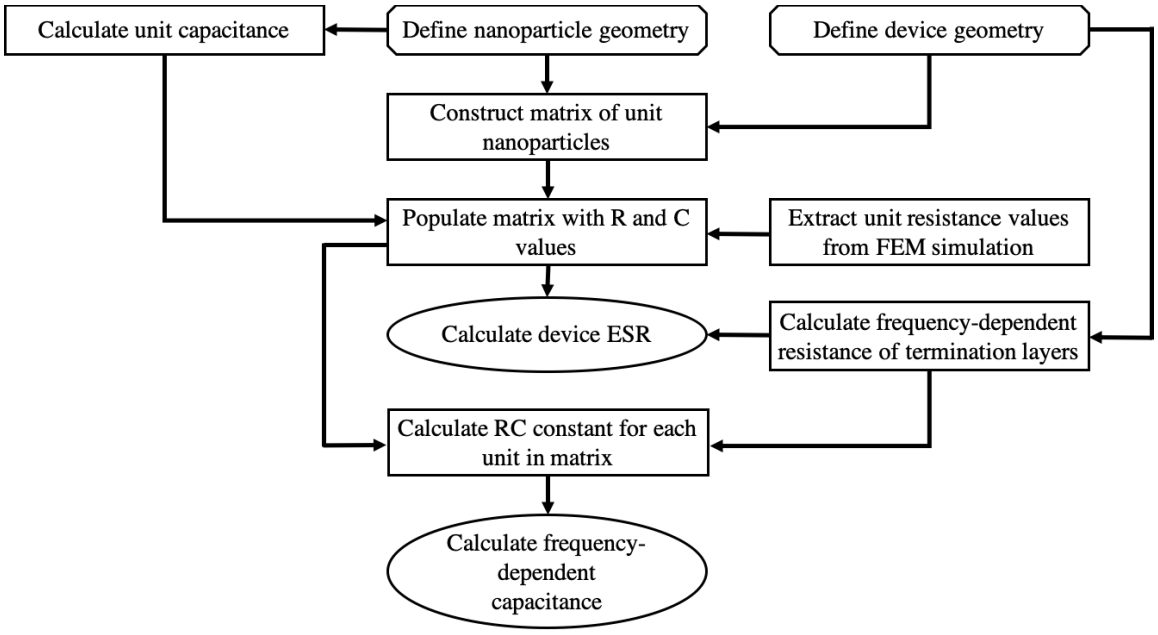


Figure 25. Process flow for construction of capacitance and ESR model

3.1.3 Capacitor Characterization and Measurements

To validate the model, the modeled electrical characteristics are compared to the measured frequency response of a real nanoparticle-based capacitor. A tantalum capacitor is used for comparison, which consists of a tantalum nanoparticle anode, a Ta_2O_5 dielectric, and a PEDOT:PSS conducting polymer cathode. The fabrication process used to form the capacitor will be described in CAPACITOR FABRICATION AND PROCESS DEVELOPMENT. The particle geometry, dielectric thicknesses, and the thickness of the conducting polymer were measured using scanning electron microscopy (SEM). The surface area and of the sintered nanoparticle structure was measured using Brunauer-Emmett-Teller (BET) surface area analysis. The electrical performance of the capacitors was measured using an Agilent 4294A Precision Impedance Analyzer.

3.2 Results

The results from FEA simulations are included in Figure 26. The effect of particle size, conducting polymer coating thickness, and degree of sintering (defined by k_{sint}) were all studied. Resistivity values of 1.3×10^{-7} $\Omega\times$m and 2×10^{-5} $\Omega\times$m were used for the tantalum and conducting polymer resistivity, respectively. Based on the FEA results, there is a clear power law relationship between the tantalum nanoparticle resistance along its length and the nanoparticle diameter due to the reduction in cross-sectional area (Figure 23b). The relationship found shows $R_{anode} \propto R_{core}^{-1}$, as expected. Additionally, resistance is reduced as the coarsening process from sintering proceeds. Shorter particle length, and thicker neck regions helps to prevent current crowing and choking through the neck between particles. The effect of k_{sint} on nanoparticle resistance is exasperated at smaller nanoparticle sizes, since the increase in cross-sectional area of the neck region is more extreme for larger particle sizes.

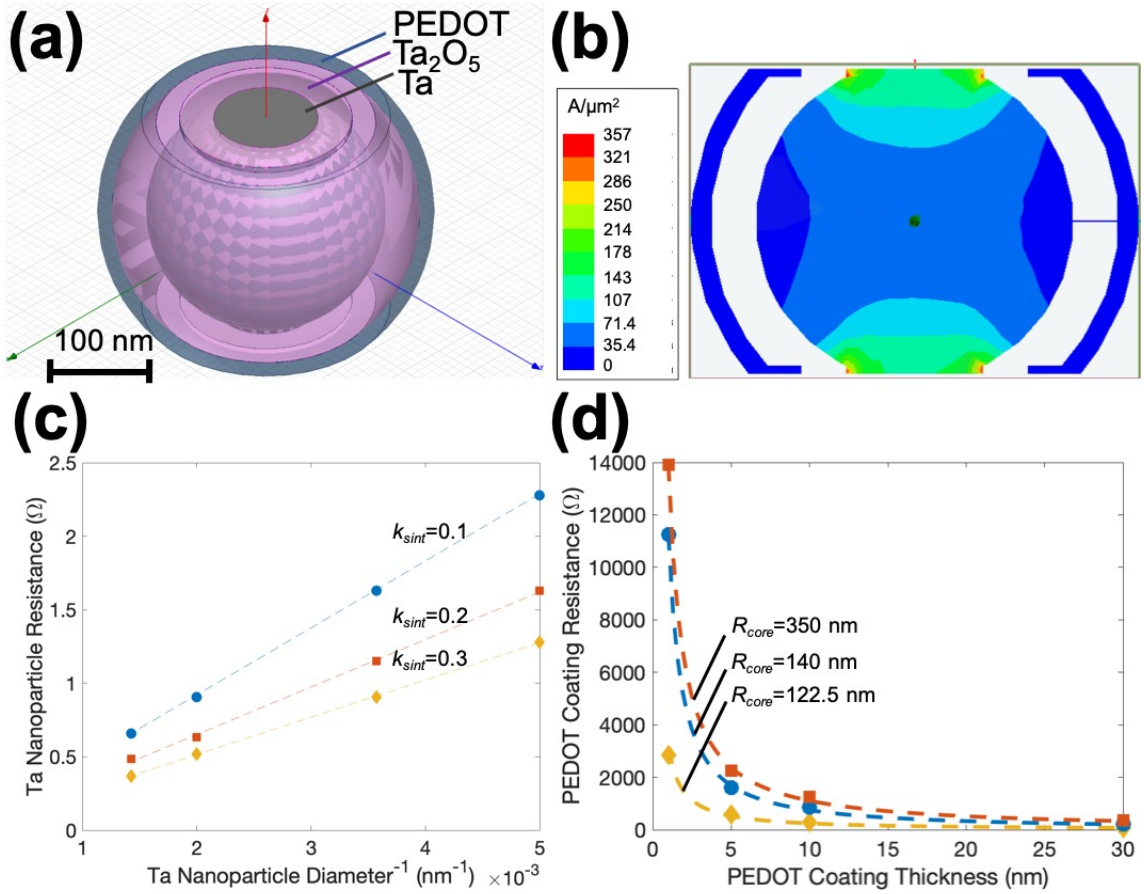


Figure 26. (a) Geometry used in FEA DC conduction simulations of tantalum-PEDOT:PSS nanoparticle-shell (b) Current density through cross-section of nanoparticle with Ta core radius of 122.5 nm and a 15 nm thick PEDOT coating, when a 3 V bias is applied across the ends of the nanoparticle (c) Effect of nanoparticle size and degree of sintering on nanoparticle resistance (c) Effect of PEDOT coating thickness and nanoparticle size on the coating resistance

In Figure 26d, a power law relationship is again seen between the PEDOT:PSS conducting polymer coating resistance and the PEDOT:PSS thickness. For a 280 nm particle size, it was found that $R_{cathode} \propto t_{outer}^{-1.18}$. Shown in Figure 26b, the same voltage applied across the tantalum nanoparticle and conductive polymer coating will result in much larger current densities through the tantalum. This is indicative of the much higher resistance in the PEDOT coating, which dominates the ESR of the capacitor. It is important to note that the conducting polymer thickness is not uniform throughout the nanoporous structure, due to the inability to completely infiltrate the nanostructure with conducting

polymer during the cathode deposition process. The nanoparticles nearest to the nanoporous surface exhibit a thick polymer coating, while the ones furthest from the surface show very thin coating thickness. By fitting a curve to the FEA measurements, the values of cathode resistance elements in the equivalent circuit could be adjusted to account for a varying conducting polymer thickness along the branch length. This is accounted for in the model by assuming a linear distribution of coating thickness from the top to bottom nanoparticle and adjusting the values of the resistance elements along the nanoparticle branches according to the power law relationship obtained in Figure 26c.

To verify the model, comparison to measured capacitance and ESR values of a real tantalum capacitor at various frequencies was needed. SEM images of the tantalum capacitor used are included in Figure 27. Real values for particle size, oxide thickness, conducting polymer thickness, k_{sint}, capacitor height, capacitor area, and BET surface area density could be obtained and are included in Table 5. While the surface area density is not an input parameter in the model, it could be calculated in the model based on the particle size and degree of sintering. The calculated value of 1.2 mm^2/g of sintered nanomaterial shows good agreement with the BET surface area measurements of 1.2-1.5 mm^2/g. The resistivity values were obtained from data sheets.

Table 5. Parameters used in capacitance and ESR model based on measurements obtained from an actual tantalum capacitor

Model Parameters	Input Values
Lateral Area (mm^2)	5
Vertical Height (μm)	50
Nanoparticle Diameter (nm)	300
k_{sint}	0.05
Surface Area (mm^2/g) (Measured/Calculated)	1.2-1.5/1.2*
Oxide Thickness (nm)	35
Oxide Relative Permittivity	23
Dissipation Factor	0.025
Tantalum Resistivity (Ω×m)	1.3×10^{-7}
PEDOT:PSS Thickness (nm) (Surface/Bottommost Interior)	15/1
PEDOT:PSS Resistivity (Ω×m)	2×10^{-5}
$k_{snaking}$	4
Graphite Resistivity (Ω×m)	1.15×10^{-4}
Ag Paste Resistivity (Ω×m)	2×10^{-6}
Contact Resistance (mΩ)	5

*The surface area value normalized by nanoparticle mass is calculated after model construction of nanoparticle geometry and used to verify the geometry in the model. It is not used as a model input parameter.

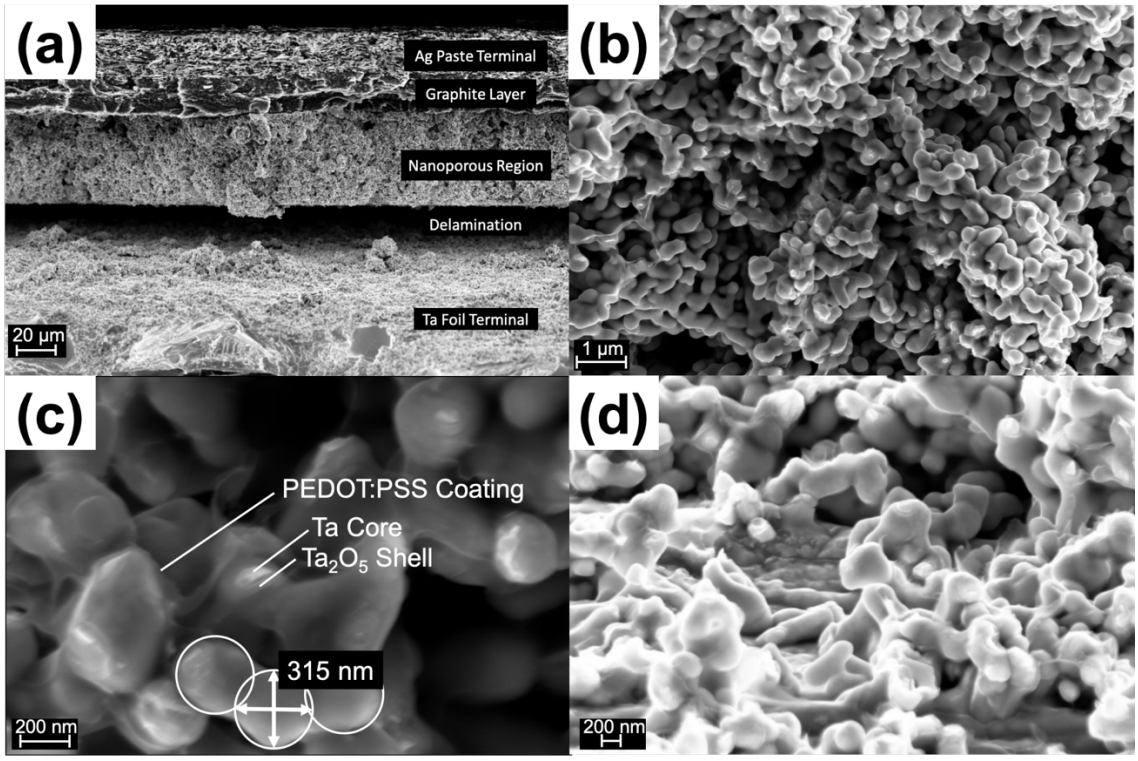


Figure 27. (a) SEM image of SEM cross-section of tantalum nanoparticle capacitor, with Ta foil anode terminal and graphite/silver paste cathode terminals below and above the nanoporous region of the capacitor (b) Internal nanoporous structure of capacitor populated with nanoparticles and pores (c) Various layers forming nanoparticle, with diameter and approximated overlapping spheres shown for the nanoparticles (d) Bottom of nanoporous region near Ta carrier foil, furthest from surface, showing very thin conducting polymer coating, if any.

Using the parameters obtained from SEM imaging, the predicted frequency response of the capacitors was compared to the measurements obtained from the real capacitor. The fitting parameter k_{snake} was used to account for porosity in the system. A k_{snake} value of 4, or branch length that is 4× the height of the capacitor is reasonable for the amount of porosity in the system, but the true value cannot easily be obtained from simple SEM imaging. The predicted capacitor performance shows good agreement with the measured capacitance and ESR versus frequency (Figure 28). While the Elmore's delay method is good for predicting when the roll-off begins, it vastly under predicts the rate at which roll-off occurs as frequency continues to increase. In contrast, the branch

capacitance method and hybrid method show only slightly greater roll-off than the measurement, with the predicted roll-off using the hybrid method being slightly lessened.

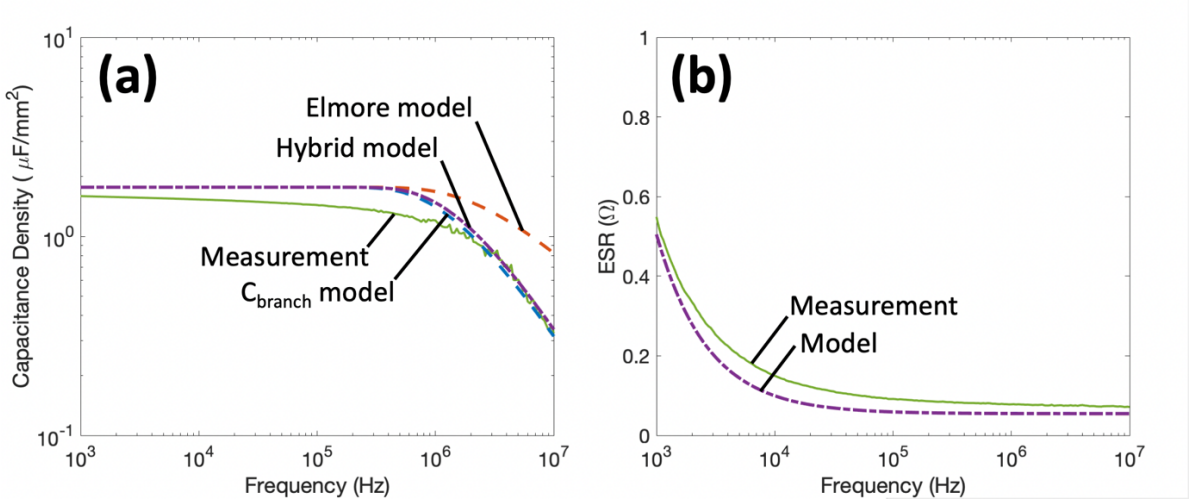


Figure 28. Simulated and measured capacitor performance versus frequency, including (a) capacitance density and (b) ESR. All three methods for calculation of RC delay are included.

ESR is calculated the same way regardless of the method used for RC constant calculation, and remains largely unaffected by the method used. Again, good agreement is seen between the model and measurement. The results indicate that the hybrid method can be used to accurately model and predict the electrical performance of tantalum capacitors based on their nanostructure.

Figure 29 shows how the predicted RC constant of each branch within the nanostructure varies along the height of the capacitor. At the top capacitor surface, the conduction length through the cathode is much shorter than through the anode. At the bottom of the anode structure, near the tantalum carrier foil and terminal, the opposite is true. Since the resistance in the capacitor is dominated by the cathode material, the RC time constants near the surface of the capacitor structure are much smaller than those that are deep within the internal nanostructure. By reducing the RC constants of the

nanoparticles near the bottom of the capacitor structure, the capacitance can be made to remain stable up to higher frequencies.

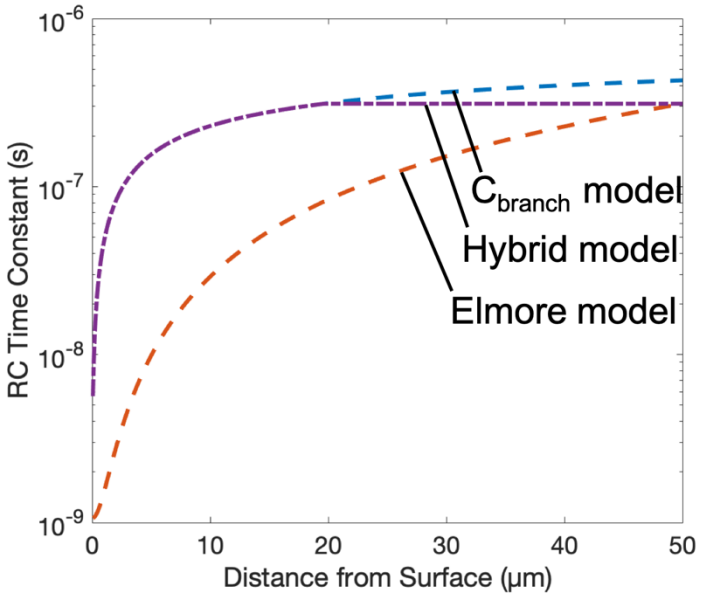


Figure 29. Calculated relationship between RC time constant and nanoparticle distance from the upper surface cathode for the measured capacitor based on simulation results

With the model validated, predictions can be made about the impact of capacitor nanostructure on electrical performance. The first structural effect studied was that of the conducing polymer coating thickness (Figure 30). Both the capacitance stability and ESR can be improved by using a thicker and more uniform polymer coating.

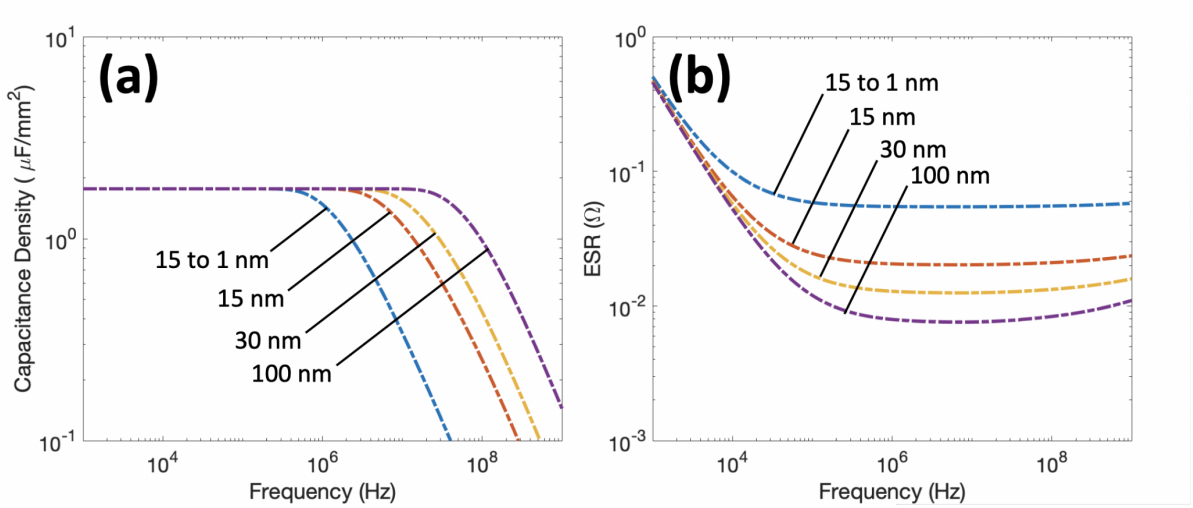


Figure 30. Predicted effect of PEDOT conducting polymer cathode thickness on (a) capacitance density and (b) ESR of a 50 µm thick, 300 nm core particle size tantalum capacitor, using the hybrid model to calculate the RC delays, where the 15 to 1 nm thickness represents a linear reduction in thickness from the surface nanoparticles to the most interior ones. Other than the PEDOT thickness, the model parameters are unchanged from Table 5.

A reduction in capacitor height was also shown to have similar effects on the capacitor's electrical performance (Figure 31). Since by reducing the capacitor height the branch length is reduced, the elements with larger RC time constants are removed from the system. This results in improved frequency and reduced ESR contribution from conduction resistance. The effect of capacitor lateral area was also studied (Inset of Figure 31b). The ESR is also reduced with larger areas due to a greater number of parallel branches.

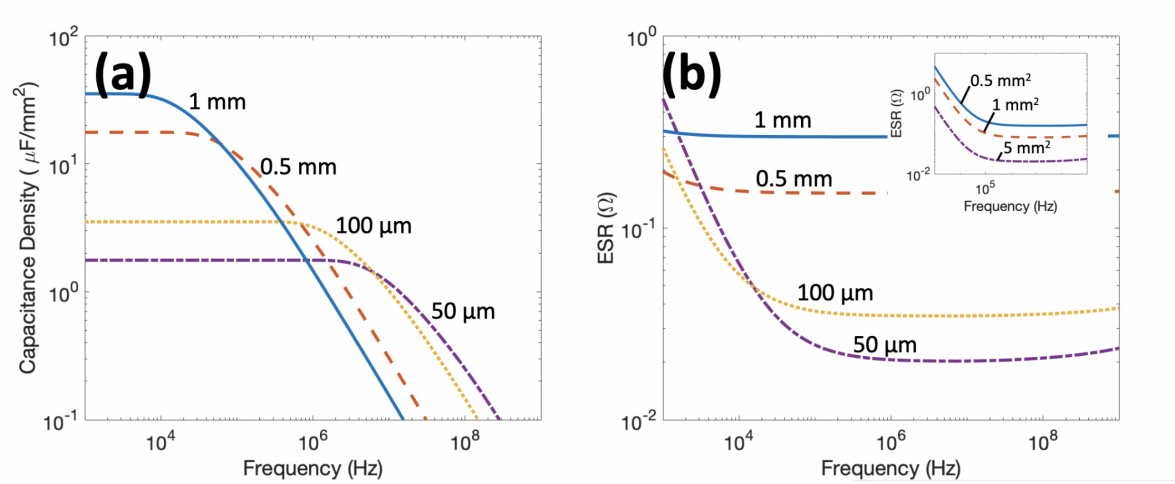


Figure 31. Effect of the height of the nanoporous region in the capacitor on (a) capacitance density and (b) ESR (Inset: Effect of capacitor lateral area on ESR), assuming a conformal 15 nm thick coating of PEDOT on the nanoparticles. Other than the capacitor height or area and PEDOT coating thickness, the model parameters are unchanged from Table 5.

Finally, the effect of replacing the conducting polymer cathode with a titanium nitride (TiN) cathode was predicted using the hybrid model. TiN is a low-resistance, metallic-like material that can be deposited using ALD to uniformly coat the nanoparticles. By replacing the cathode material with TiN, the resistivity can be reduced by almost an order of magnitude. The resistivity of TiN is only ~4.3×10^{-6} Ω×m [68], much lower than the 2×10^{-5} Ω×m resistivity of PEDOT. The result of using a uniform 15 nm thick TiN coating instead of a uniform 15 nm PEDOT coating is included in Figure 32.

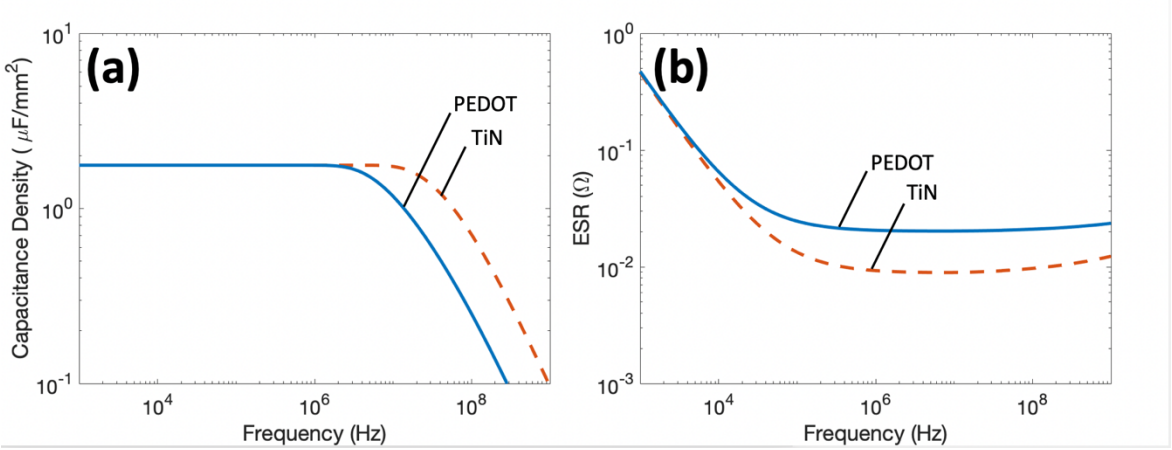


Figure 32. (a) Capacitance density versus frequency and (b) ESR versus frequency when 15 nm coatings of PEDOT or TiN is used as the cathode material. Other than the cathode material and thickness, the model parameters are unchanged from Table 5.

3.3 Discussion

Verification of the model's accuracy was achieved through the comparison with both circuit simulation and then a real capacitor system (Figure 28). Using the hybrid method, the effective RC time delay for charging and discharging the capacitor provided by each nanoparticle could be calculated without the use of complex circuit simulations. Taking advantage of this, the model could then be compared to measurement of a real system with thousands of elements. The predicted low-frequency capacitance density is only slightly higher than what was measured, which is reasonable since it is safe to assume not every single nanoparticle is completely coated in conducting polymer [69]. The roll-off frequency, where the capacitance begins to drop off dramatically, is just below 1 MHz, and is consistent with what was measured.

In terms of ESR, there are two regions in the curve. At lower frequencies, the ESR continues to drop. This is inherent to the ESR caused by dielectric loss, captured in Equation 20. However, the simulated drop in ESR occurs slightly faster than what was measured. This can be attributed to the fact that the dissipation factor (DF) generally increases with frequency in a real system [23]. In the model, the DF is assumed to be

constant. Thus, the measured drop in ESR occurs more slowly than the model predicts. At higher frequencies, the ESR is dominated by the contribution of conduction resistance through the electrodes. The values predicted by the model are very similar to what was measured, and only slightly lower at 10 MHz. The slight difference could be due to the contact resistance value of 5 mΩ used in the model being too low, since the contact resistance between conducting polymer, graphite, and silver paste layers is not accounted for. Additionally, the resistivity values used in FEA simulations may have been lower than that of the materials in the real system.

From Figure 29, it is clear that the conducting polymer cathode is the dominant contribution to the resistance in the RC constant of the capacitor elements. The resistivity and cross-sectional area of the polymer coating is much smaller than the nanoparticles, so this is expected. Therefore, to improve the frequency stability and ESR of the capacitor, the cathode coating should be the focus of material and process development. A better infiltration process to improve the coating thickness can drastically improve capacitor performance, as seen in Figure 30. It is evident from Figure 30a that improvement in coating coverage so that it is thicker and more uniform throughout the structure can improve the frequency stability of the capacitor by orders of magnitude. By making the coating uniform and increasing the maximum thickness from 15 to 30 nm, the roll-off frequency increases from just below 1 MHz to just below 10 MHz. Figure 30b shows there is a significant reduction in ESR at higher frequencies with increased coating thickness. The low frequency ESR is largely unchanged, since this portion is still dominated by the dielectric loss.

Another option to improve capacitor operation to the MHz regime is by reducing the distance between anode and cathode terminals. While a capacitor with a 1 mm height, or 1 mm distance between anode and cathode terminals, is only stable until ~10 kHz, a 50 μm distance improves the frequency stability up to ~1 MHz (Figure 31). This means an

improvement of ~2 orders of magnitude. While the capacitance density does increase with height, the volumetric density in terms of $\mu F/mm^3$ remains largely unchanged. At the same time, increasing capacitor area helps to reduce the high-frequency ESR (inset of Figure 31b). While the capacitance density is not affected by area, the ESR is due to the total number of parallel branches, and thus parallel resistance elements, changing with area. Therefore, more planar capacitor structures integrated into the electronic packages in 3D can be used in high-performance power converter systems to meet the needs of next-generation computing.

Finally, the material system can be changed to improve the capacitor's electrical properties. By replacing a PEDOT:PSS coating with TiN as the cathode material, an order of magnitude improvement in frequency stability and ~50% reduction in high-frequency ESR can be achieved (Figure 32). Thus, advanced deposition processes with new materials can also help pave the way for advanced capacitors in future power distribution networks.

3.4 Summary

In summary, a model has been developed that can accurately that can accurately predict the relationship between capacitor nanostructure and electrical performance, allowing for optimization of nanostructure to reach closer to the theoretical limits of device performance. The accuracy of the model is demonstrated by characterizing a real tantalum capacitor device and comparing the predicted capacitor performance to the measured performance. The model then studies the effect of capacitor materials and device geometry on the bulk electrical characteristics of the device, including capacitance density, frequency stability, and ESR. It is shown that by using an ultra-thin structure of <100 μm in conjunction with low-resistance cathodes deposited uniformly,

the capacitance density of >1 μF/mm^2 can be pushed well beyond 10 MHz, enabling their use in high-switching-frequency power converters. The next chapter will focus on the development of process to fabricate such a structure.

CHAPTER 4: CAPACITOR FABRICATION AND PROCESS DEVELOPMENT

The objective of this chapter is to develop a process to fabricate the ultra-thin, high-density tantalum capacitors. Tantalum capacitors are unique in that they combine a high electrode surface area with a relatively high permittivity dielectric (ε_r of ~22-25) to provide some of the highest densities available in capacitor technology today [24]. Unlike the thick ceramic dielectrics used in MLCCs, a tantalum pentoxide dielectric (Ta_2O_5) can be galvanically formed to nanometer-scale thicknesses, so that high capacitances at low voltages can be obtained [70]. Additionally, Ta_2O_5 dielectrics are paraelectric, providing a relatively stable permittivity (and thus capacitance) with changes in temperature, which is especially important for high power levels and in embedded components near active dies where temperatures can become much higher than for on-board components [66].

The drawback, however, is that tantalum capacitors are formed from pressed tantalum pellets, which is sealed in casing. Due to this, the smallest form factors available are >0.5 mm thick with much of the volume going to casing rather than active electrode area. Additionally, due to the high-surface area nanostructure, there exists a long electrical path-length from electrode to terminal that results in significant resistance during charge/discharge and inferior frequency stability. Even the most advanced terminal designs can only achieve frequency stability up to around 300 kHz before a significant capacitance drop, falling short of the 1-10 MHz switching frequency needed in emerging power-conversion systems. In this chapter, a novel tantalum capacitor design using a printed anode structure is presented that allows for on-chip or on-package integration. The capacitors not only improve the density of existing technology, but also achieve capacitance stability beyond 1 MHz due to their ultra-thin design. As discussed in

CAPACITOR DESIGN, superior electrical performance can be obtained by using a thin-film architecture for the anode.

A process is presented to fabricate thin-film tantalum capacitors with improved frequency stability and reduced ESR. Capacitors are demonstrated with capacitance stability of >1 μF/mm^2 beyond 1 MHz while maintaining a form factor of <100 μm thickness. The capacitors are fabricated with a low-cost, scalable process and achieve low ESR of <50. The fabrication process is studied, including the anode printing, dielectric formation, and cathode deposition. The entire process is depicted in Figure 33. Finally, the electrical characteristics of the thin-film tantalum capacitors are measured, and then compared to commercial tantalum capacitors that exist today.

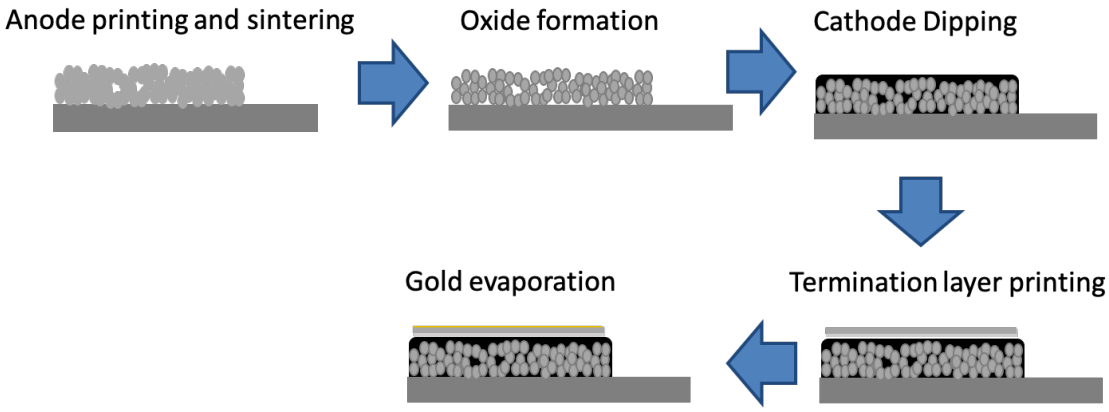


Figure 33. Thin-film tantalum capacitor fabrication process

4.1 Methods

4.1.1 Anode Printing

Porous tantalum anode arrays were acquired from H.C. Starck Inc. The anodes were printed as a slurry paste composite with tantalum nanoparticle inclusions on a 25 μm thick tantalum foil carrier. The printed anode area can be easily modified, making the process both resilient and scalable to any design need and providing integration directly

on any substrate of choice. However, in this research, an area of 5 mm^2 was chosen. The arrays were then dried and sintered under forming atmosphere to obtain a continuous, high-surface area anode structure with controlled porosity and high tantalum purity while minimizing the formation of any metallic oxides (Figure 34). During the drying step, the nanoparticles were debindered and a resulting solvent weight loss of 18-20 % occurred.

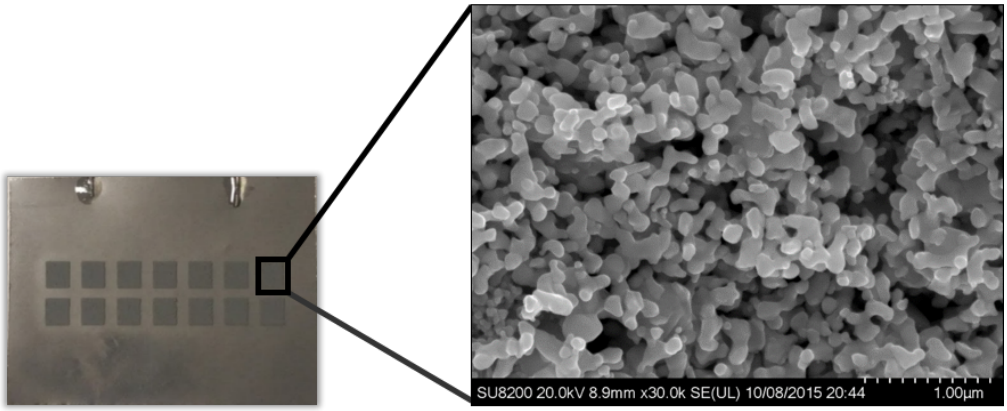


Figure 34. Tantalum carrier foil with printed capacitor anode array consisting of 5 mm^2 regions of 50 µm thick, porous tantalum (enlarged SEM image showing sintered tantalum nanoparticles that populate the porous regions)

The paste was sintered at 1310° C-1400° C for 15 minutes, depending on the initial nanoparticle size and desired degree of sintering. This is slightly under ½ the melting temperature of tantalum to encourage solid-state diffusion and the formation of necks between particles. It is important to provide enough temperature and time that sufficient thickening of neck regions occurs and a continuous complex is formed, but not so much time that the pores become too small and surface area is overly depleted. The average tantalum particle size can be varied depending on the application need. The particles should be large enough to support the oxide that will be formed onto them, but not so large that the surface area is reduced. Additionally, the impedance of the structure will vary significantly depending on the particle size, so that should also be considered. In this

thesis, particles with diameters ranging from 150 nm to 700 nm were studied. The particle sizes were measured using SEM imaging.

The resulting surface area enhancement within the 50 μm thick anode structure can be estimated from the wet capacitance measured at 100 Hz. Knowing the dielectric permittivity and the dielectric thickness, the surface area can be estimated using Equation 2. If the capacitance is measured using a wet electrolyte cathode so that all the electrode surface area is accessed by the electrolyte, and the permittivity and thickness of the dielectric is known (in this case, the Ta_2O_5 was measured to have a dielectric constant of ~22, which agrees with literature), then the electrode area can be calculated. To do this, a high surface area stainless steel counter electrode was used to make good electrical contact between the LCR meter and the 0.05 M H_2SO_4 electrolyte cathode (Figure 35). Using particles with a 285 $\pm$ 37 nm diameter, a surface area density of roughly 88,000 cm^2/cm^3 is obtained. Alternatively, the surface area can be measured directly using BET surface area analysis. In this case, a surface area of 88,300 cm^2/cm^3, showing good agreement between the two measurement methods. For a 700 nm particle size, the surface area was calculated to be ~34,000 cm^2/cm^3 using wet capacitance measurements. Since the particles are larger, they cannot be packed as tightly into the same volume, resulting in reduced surface area density. This results in ~2.6$\times$ area enhancement using a 285 nm particle size versus a 700 nm particle size. The surface area enhancement predicted by the model described in CAPACITOR DESIGN is ~2.9$\times$, so again there is good agreement between the various measurement or calculation methods. After obtaining high surface area anode structures, the next step in the fabrication process is dielectric formation.

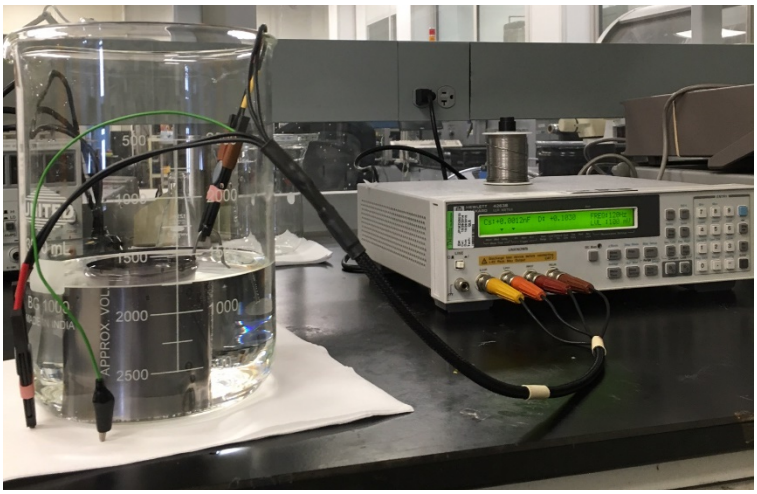


Figure 35. Experimental setup used for obtaining capacitance measurements of the tantalum capacitor array using a liquid electrolyte cathode

4.1.2 Dielectric Formation

After anode printing and sintering, a scalable fabrication process must be developed to form the rest of the capacitor. Dielectric formation is carried out using an established electrochemical process of anodization. Growth of amorphous Ta_2O_5 is important for low leakage current, as grain boundary defects are known to provide shallow electron traps for Poole-Frenkel emission across the oxide layer, which results in a capacitor with high leakage current [28, 32]. Defects and impurities also contribute to high leakage currents and premature dielectric breakdown [71]. Additionally, high control and uniformity is important for maximizing capacitance and dielectric break down voltage. This can all be monitored and controlled using anodization, with many experimental knobs that can be adjusted and the ability to monitor the total charge transfer during the oxide growth process. Conditions such as temperature, agitation of electrolyte, concentration of electrolyte, etc. can be adjusted to optimize the growth conditions. Various techniques will be used to characterize the oxide layer, including electrical measurements and SEM imaging.

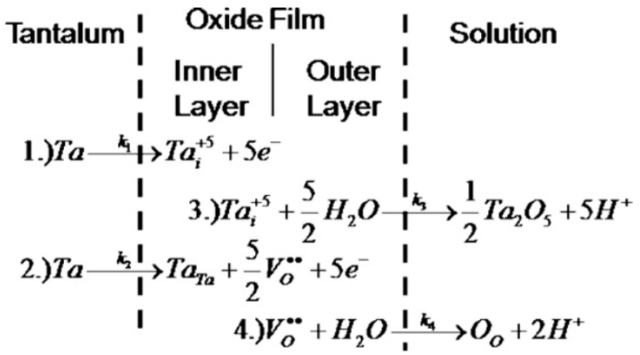


Figure 36. Proposed point defect model of tantalum pentoxide growth in an acidic electrolyte [72]

Dielectric formation was carried out using standard anodization process in a 0.1 M H_3PO_4 electrolyte solution with a stainless-steel counter electrode. The anodization was carried out at 85° C, which has been shown to result in the growth of amorphous Ta_2O_5 [70, 72]. The experimental setup used to do this is shown in Figure 37, where both the voltage and current are monitored separately from the power source for greater accuracy and control.

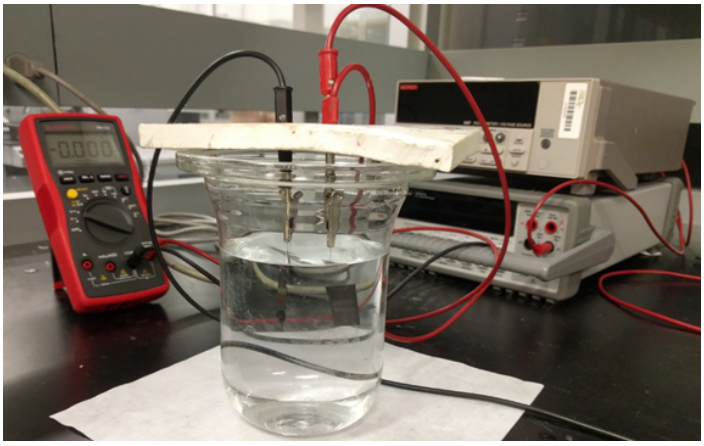


Figure 37. Experimental setup used for anodization of the tantalum anode and growth of amorphous tantalum pentoxide

A steadily increasing voltage was applied at a rate of 0.005 V/s until a final formation voltage ($V_{formation}$) was reached (Figure 38a). Then, $V_{formation}$ was held until the current dropped below 50 µA during anodization dwell (Figure 38b). The slow ramp-rate is used to ensure conformal oxide formation with minimal defects. This procedure was also followed using higher formation voltages and larger particle sizes (Figure 39). The charge transfer during this process provides insight into the growth of the oxide layer. A flat curve after the initial current spike indicates steady-state, conformal oxide growth without too many defects or impurities, which is important for low leakage current. In general, galvanostatic anodization is preferred as it provides more conformal oxide growth [70, 72]. The initial current spike is attributed to the large dV/dt (change in voltage with time) to begin the process, that eventually settles to a steady state. The differences in steady-state current between samples with the same particle size is attributed to small differences in the electrolyte chemistry, or pH, which affects the electrolyte charge-transfer ability, as well as small difference in the surface area of the anode (and how much of the sample was immersed in the electrolyte). However, there is a much larger difference in steady state current between samples with different particle sizes, due to the differences in the surface area.

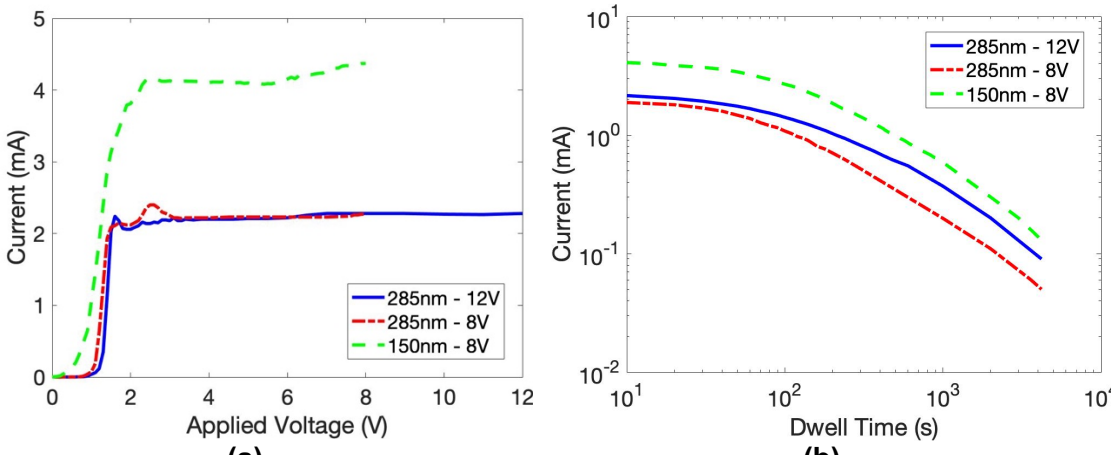


Figure 38. (a) Current measured during anodization (a) ramp to formation voltage (0.005 V/s) and (b) anodization dwell

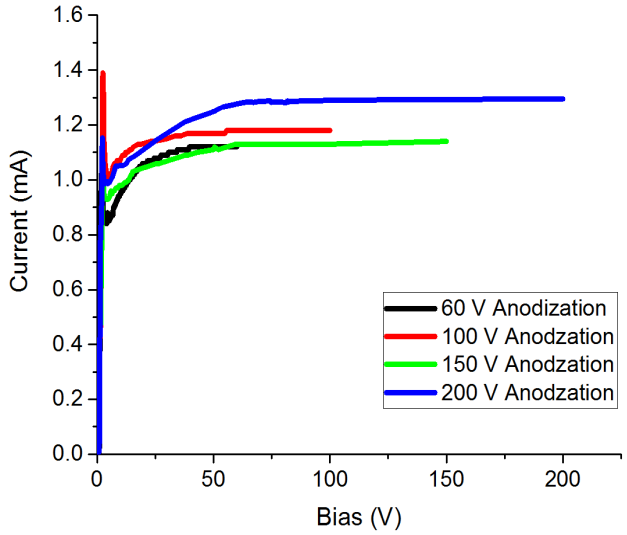


Figure 39. Anodization ramp (0.005V/s) using larger 700 nm tantalum particle size

4.1.3 Cathode Deposition

Thereafter, conducting polymer cathode was impregnated into the porous, anodized tantalum using a vacuum-assisted, cathode dipping process. The capacitor arrays were dipped into suspensions of polymerized PEDOT:PSS of varying viscosity a total of nineteen times under vacuum. After each dip, the arrays were placed in an oven at 120° C for five minutes to evaporate the solvent and provide a conductivity of ~500 S×cm. Thick polymer coverage as a cathode is imperative in Ta capacitors as it prevents current choking points and helps maintain low ESR. Therefore, lower viscosity solutions are used initially to help impregnate the deeper regions within the porous structure, followed by more viscous solutions in the upper layers. Patterning by subtractive etching or lift-off methods was used to selectively deposit the cathode in the porous tantalum regions, and not on the tantalum carrier foil itself.

In the final steps, an electrically conductive graphite and silver paste layers are applied that act as diffusion barrier and current collector respectively. The diffusion barrier is needed to prevent migration of silver ions to the dielectric. Ion impurities within the Ta_2O_5 dielectric are known to create shallow electron-traps that allow Frenkel-Poole emission across the oxide leading to increased leakage current [15]. The silver paste layer acts as a current-collecting layer and provides low contact resistance to electrical interconnects. The thickness of 100 μm can be further reduced by optimizing the current collector layer thicknesses. This can include direct metallization using evaporated Ti/Au like layers. For this study, traditional C/Ag layers are used as current collectors.

4.1.4 Electrical Measurement and Testing Methods

The capacitors' electrical characteristics were measured across broad frequency range. For the wet capacitance measurements conducted at 100 Hz, a Hewlett Packard 4263B LCR meter was used at 100 mV DC bias. The capacitance and ESR were also measured from 1 kHz to 10 MHz using an Agilent 4294A Precision Impedance Analyzer, also under a slight DC bias of 100 mV.

4.2 Results and Discussion

A cross-sectional image of the capacitor nanostructure after each step in the fabrication process is included in Figure 40. In this case, the ~285 nm sintered tantalum nanoparticles can be seen in Figure 40a. While some regions are populated with large pore sizes, others show highly dense packing of nanoparticles. In Figure 40b, the cleaved dielectric shell of tantalum pentoxide can be seen surrounding the nanoparticles. Here, a formation voltage of 20 V is used to produce a thicker oxide coating, although the thickness can be controlled down to <10 nm. In this case, however, the oxide almost completely

grows into the thinner neck region between tantalum particles. If this occurs, parts of the anode will become completely oxidized or shut off from electrical connection from the rest of the capacitor, thus being detrimental to the total capacitance that can be obtained. For this size nanoparticle, a $V_{formation}$ of 20 V is the safe limit. in Figure 40b, a thick coating of conductive PEDOT:PSS can be seen surrounding the particles. Some regions of the nanostructure showed coating thickness up to 20 nm, while other regions showed a coating that was almost nonexistent. Finally, the complete capacitor structure is shown in Figure 40d, including the solid tantalum, nanoporous tantalum, graphite, and silver paste layers. The nanoporous region is shown to have a thickness of only 50 µm, while the entire capacitor is <100 µm thick.

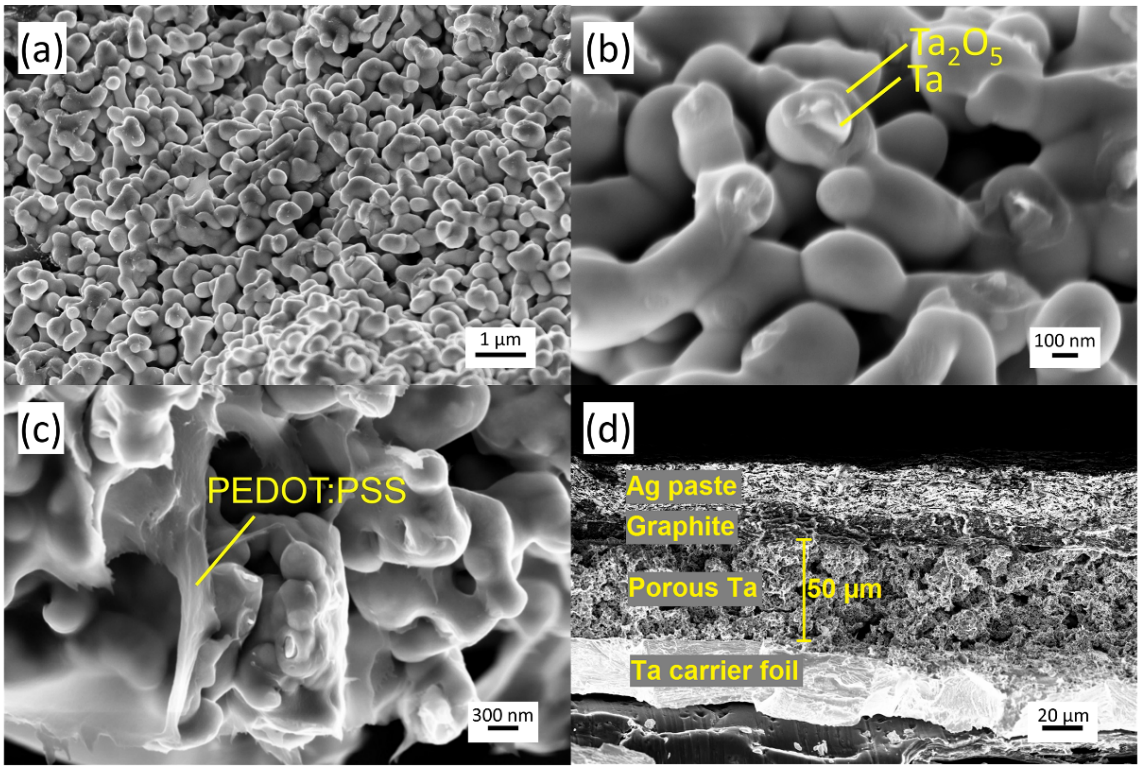


Figure 40. (a) Tantalum nanoparticles comprising the capacitor anode (b) Oxide shell formed around the tantalum nanoparticles after anodization (c) Conducting polymer coating surrounding the particles after cathode dipping (d) Final cross-section of the capacitor structure after deposition of termination layers

The final formation voltage during anodization was varied to test the effect on the nanostructure and electrical properties. Several capacitors were formed at 6 V, 8 V, 12 V, 60 V, 100 V, 150 V, and 200 V for operation at 2-48 V or higher. In an IVR, higher conversion ratios are desired. A decoupling capacitor is needed that can handle high voltage power lines at the input. A thicker dielectric layer, and thus a larger higher formation voltage, is needed to protect the oxide from dielectric breakdown, which can occur when too large of an electric field is applied across the dielectric. Dielectric breakdown, or formation of conductive paths across the dielectric, can occur due to avalanching, thermal runaway, defect formation, electromechanical collapse, among other reasons [32]. Therefore, a large range of formation voltages were studied.

The tantalum pentoxide thickness was measured for various samples using SEM and confirmed with wet capacitance measurements, and a linear relationship with the formation voltage was found (Figure 41). The relationship of 2.26 nm/V is only slightly higher than previous results, which is attributed to the longer dwell times used in this paper [5]. Thicker dielectrics are needed for higher-voltage operation to prevent dielectric breakdown [16]. According to the relationship found between oxide thickness and formation voltage, anodization to 6 V, 8 V, and 12 V should result in oxide thickness of roughly 18 nm, 22 nm, and 31 nm, respectively. Higher formation voltages of 40-200 V result in oxide thickness up to 440 nm.

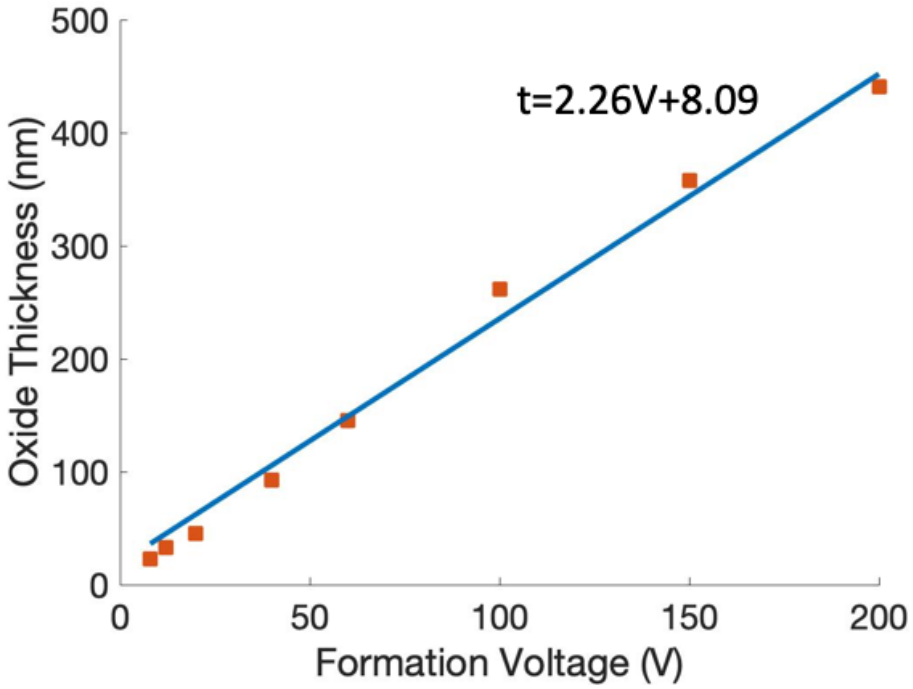


Figure 41. Linear relationship between formation voltage and tantalum pentoxide thickness

The linear relationship between oxide thickness and formation voltage was confirmed with capacitance measurements (Figure 42). The average capacitance was recorded for each formation voltage, and a relationship between capacitance and formation voltage was obtained. If one assumes a linear relationship between $V_{formation}$ and dielectric thickness, then the capacitance should decrease with increasing $V_{formation}$ according to a power law relationship as predicted by Equation (2). This is the relationship found for the capacitors tested ($R^2 > 0.99$). By adjusting $V_{formation}$, the capacitors can easily be tuned to meet a desired application need. It is important to realize that while these volumetric densities are large, they do not consider the volume used up by the termination layers that make up the rest of the capacitors, and only consider the volume of the nanoporous regions. If the termination layers are considered in the volume calculations, the thickness becomes ~100 μm rather than 50 μm, so the volumetric densities are roughly

halved. Even then, these capacitance densities are quite large compared to existing capacitor technologies.

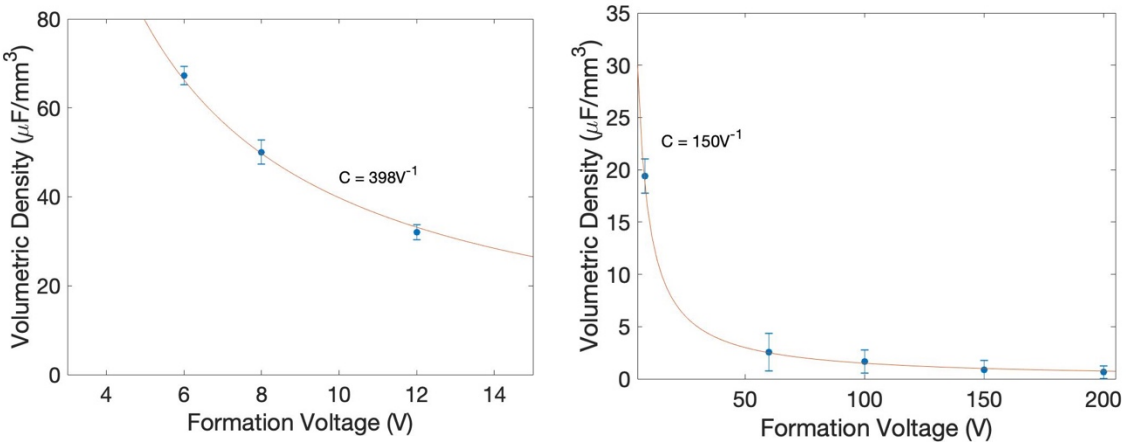


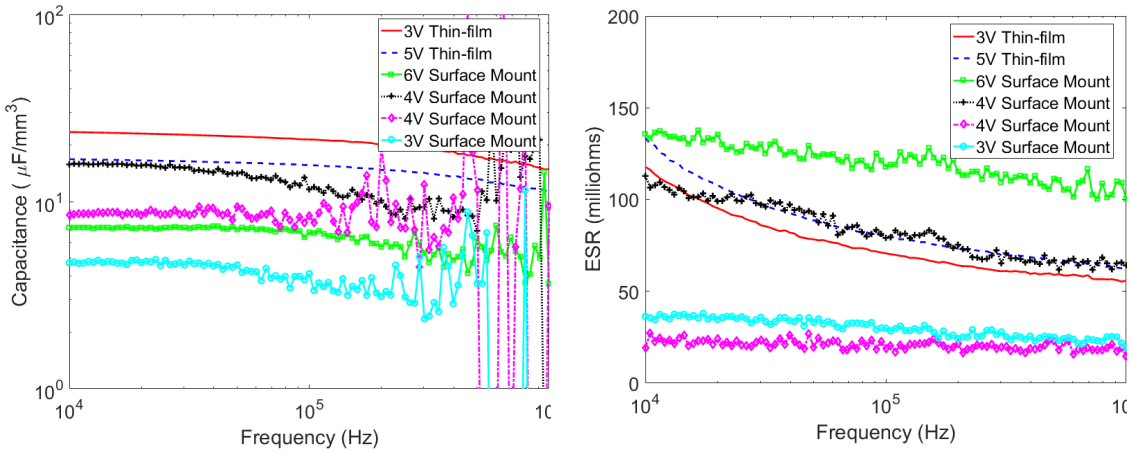
Figure 42. Inverse power law relationship between formation voltage and volumetric capacitance density with (a) 285 nm tantalum particle size and (b) 700 nm tantalum particle size, considering only the volume of the 50-μm thick nanoporous region. When the entire capacitor thickness is considered, including the termination layers, the resulting volumetric density is roughly half of what is shown

The capacitor arrays were then measured across a broad frequency range after solid cathode deposition of PEDOT:PSS material, followed by graphite and silver paste printing. By comparing the capacitance using a solid versus liquid electrolyte, one can assess the degree of impregnation achieved by the solid cathode deposition process, or the amount of nanoparticle coverage achieved by the conducting polymer cathode material. In all cases, >80% impregnation or coverage was achieved. In example is included in Table 6, where the liquid-cathode capacitance of some 700 nm particle size capacitors was compared to the solid-cathode capacitance. As can be seen, at least >80% of the capacitance was achieved with the solid cathode, and that is without considering the capacitance drop that can occur between measurement at 120 Hz and measurement at 1 kHz.

Table 6. Comparison between capacitance of 5 mm^2 capacitors with an average nanoparticle size of 700 nm, measured using a liquid-electrolyte as the cathode versus solid PEDOT:PSS as the cathode

Formation Voltage (V)	Wet-Cathode Capacitance at 120 Hz (μF)	Solid-Cathode Capacitance at 1 kHz (μF)	Minimum % Coverage of Solid Cathode
8	4.85	4.44	91.5
60	0.644	0.530	82.2
100	0.411	0.333	81.0
150	0.217	0.177	81.7
200	0.160	0.139	86.9

The electrical measurements from 3 V and 5 V capacitors are compared with commercially available capacitors in Figure 43. The average volumetric density of the thin-film Ta is well above 20 μF/mm^3 (3 V) and 15 μF/mm^3 (5 V). The ultra-high volumetric density is largely attributed to the absence of a large, bulky casing. The capacitance remains relatively stable up to 1 MHz, losing less than 50% of the total capacitance across this broad frequency range. At 1 MHz, the volumetric density was above 10 μF/mm^3, with an average density of 13.54 μF/mm^3 (3 V) and 11.07 μF/mm^3 (5 V). This is the highest density ever demonstrated by tantalum capacitors, or any capacitor technology in such a small form-factor. Compared to the commercial capacitors, which also begin to resonate before 1 MHz due to higher parasitic inductance, the capacitance drops much more slowly as frequency is increased. The improved capacitance stability of the thin-film capacitors is apparent up to 1 MHz, as attributed to the reduced RC constant each of the capacitor elements. The volumetric density is also improved due to the removal of bulky casing. The ESR is also comparable to commercial capacitors, despite the much smaller form factor. This demonstrates the superiority of the new capacitor design. Table 7 is also included to further compare the commercial tantalum capacitors to those fabricated in this work.



(a) (b)

Figure 43. (a) Volumetric capacitance density versus frequency of the thin-film tantalum capacitors compared to commercial surface mount tantalum capacitors, with the operating voltage included (b) Comparison of ESR for the same capacitors

Table 7. Characteristics of low-profile solid tantalum capacitors from various manufacturers compared to the capacitors in this work

Operating Voltage (V)	Thickness (mm)	Volumetric Density 1 kHz (μF/mm^3)	Volumetric Density 1 MHz (μF/mm^3)	ESR (mΩ)
2	0.1	32.4	14.3	58
3	0.1	24.1	13.5	54
5	0.1	15.6	11.1	65
2	1.9	7.88	2.36*	40
3	1.9	5.53	1.66*	15
4	0.9	8.68	Not reported	500
6.3	0.6	11.87	Not reported	1500

**Specific values not provided, only general characteristics of the series*

Low ESR is a critical parameter for capacitors used to filter and decouple power for high-speed digital electronics. Electrode resistance is a significant component of ESR, where higher ESR indicates shorter capacitor lifetime and lower frequency response. The

increased contact area between the sintered Ta and carrier foil (also Ta) provides wider conducting paths, thus resulting in substantially reduced contribution to ESR from contact resistance. The thick and conformal polymer coating also provides low-resistance current paths through the cathode, further reducing the ESR and improving the frequency stability (Figure 43b). An average ESR of the fabricated capacitors have been measured to be <100 mΩ, with <50 mΩ at 1 MHz. Initially as the frequency increases, the ESR drops significantly as some of the internal capacitor area furthest from the terminals is lost to the faster voltage transients. This is largely due to the longer conduction path. However, there is another reason for this behavior. It is well known that resistance is inversely proportional to the cross-sectional area of the conduction path:

$$R = \rho \frac{L}{A} \tag{22}$$

where R is the resistance, ρ is the resistivity of the material, L is the path length, and A is the cross-sectional area. Therefore, it is critical to ensure a thick conducting polymer layer coats the tantalum particles to keep the cathode resistance low. However, there will always be a disparity in the polymer thickness on the outer surface to that deep within the porous microstructure. Penetration of the conducting polymer suspension becomes more difficult into the inner-most layers of the capacitor, resulting in a smaller cross-sectional area of the conduction path. Thus, resistance is dramatically increased in places where there is only a thin cathode coating. Better infiltration methods or microstructure processing can help lead to improved ESR, especially at lower frequencies.

Additionally, the capacitance of the high-voltage capacitors was also measured (Figure 44). The capacitors formed at 100 V, 150 V, and 200 V showed volumetric capacitance densities of ~1.6 μF/mm^3, 0.8 μF/mm^3, and 0.4 μF/mm^3, respectively. The frequency stability is observed to improve with increasing formation voltage, as expected due to the reduced RC constants of the internal capacitor elements.

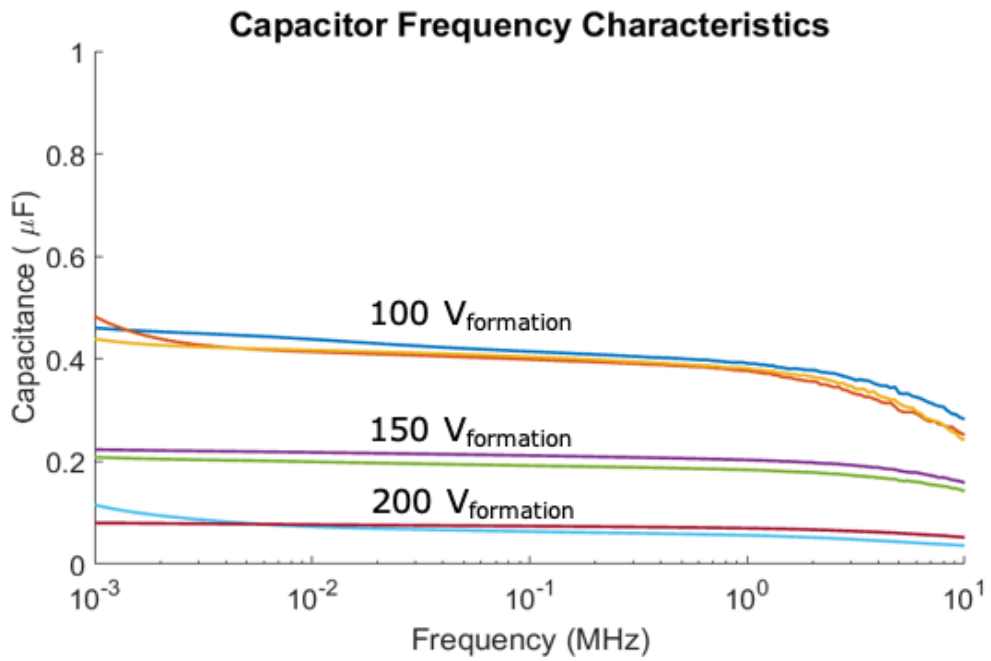


Figure 44. Capacitance versus frequency for higher voltage tantalum thin-film capacitors with 700 nm particles and 5 mm^2 area

4.3 Summary

In conclusion, by utilizing a large surface area and unique electrode structure, ultra-high density, thin-film tantalum capacitors with >10 μF/mm^3 at 1 MHz for 2-5 V operation is demonstrated for the first time with total component thickness of 100 μm. High densities of 0.4-1.6 μF/mm^3 at 1 MHz were also obtained for 30-100 V operation using a precisely controlled oxide-formation process. The improved frequency stability means the capacitors can be applied over a broad frequency range and into the MHz operating regime of emerging systems. The complete fabrication process is both low-cost and scalable. Due to the low thickness profile, the capacitor arrays can be laminated directly on a substrate or active silicon for low-footprint packaging and ultra-short interconnects for highly efficient power modules.

CHAPTER 5: 3D PACKAGE-INTEGRATION

The objective of this chapter is to develop a process to integrate the thin-film capacitors in a 3D on-package approach. One major issue with tantalum capacitors is their bulky size, which limits their ability to be integrated closer to active devices and thus improve the high-frequency switching capabilities of power converters. Due to their size, they are generally surface-mounted on-board, and far from the silicon die. Shorter interconnection lengths are necessary in future electronic systems. Such interconnections lead to reduced resistance, which improves system efficiency and reduces I^2R heating. The reduced parasitic inductance allows for higher switching frequencies before losses begin to dominate and the signal is reflected, thereby providing smoother signal.

A thin capacitor structure solves much of the issues associated with tantalum capacitors. Previously, it was shown that the frequency stability in tantalum capacitors can be improved dramatically by using ultra-thin anode structures that are printed as a paste before sintering [73]. The reduced charge/discharge current path length results in capacitors that are stable into the MHz regime, surpassing the 10-200 kHz stability of typical tantalum capacitors and allowing for use in next-generation power converters. Using a conducting polymer cathode deposited in a scalable vacuum-infiltration process, a low ESR of ~50 mΩ at 1 MHz could be attained.

Additionally, the ultra-thin structure allows for the 3D integration of capacitors directly onto silicon or silicon package, providing ultra-short interconnects and improved system performance. In the previous work, the process for capacitor fabrication was developed, and the free-standing capacitors were characterized by probing the capacitor electrodes directly. However, unlike the previous work, this work details an integration process developed for embedding and lamination of the capacitors directly on silicon

substrates, including the formation of copper vias to access the embedded capacitor electrodes. The effects of both the packaging process and copper via interconnects on capacitor performance are studied and shown to avoid any significant capacitor degradation. Using the ultra-thin tantalum capacitor technology, this chapter demonstrates the highest volumetric densities ever achieved for embedded capacitors, thus paving the way for more complex, miniaturized 3D systems.

5.1 Methods

5.1.1 Integration Process

The fabrication process for the thin-film tantalum capacitors has already been described [73]. Instead, this chapter will focus on the process that can be used to integrate the capacitor arrays directly on silicon wafers or other substrates, thus demonstrating the capability of the capacitors for 3D power converters or next-generation PDNs. The integration process is summarized in Figure 45.

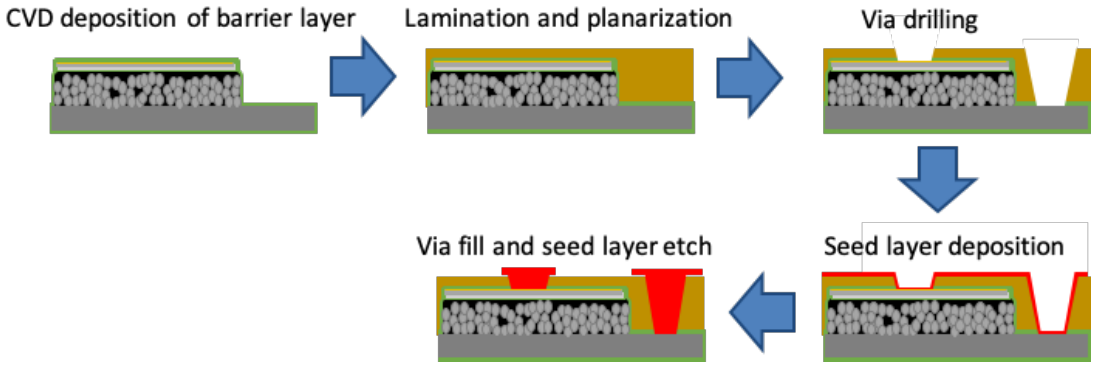


Figure 45. Summary of process used for package-integration of thin-film tantalum capacitors

Free-standing capacitors are integrated as an array using a thin tantalum sheet as

a carrier foil before lamination onto the package in a foil-transfer process. The carrier foil allows for processing of the capacitors separately before integration with the active components, including the high-temperature sintering steps that would be detrimental to other components. Since the capacitors are formed as a panel-scale array, they are kept low-cost and compatible with wafer-level packaging. However, this necessitates keeping the integration process panel-scalable. A thin gold layer is first evaporated onto the cathode and anode termination sites using a patterned shadow mask. The gold is necessary to prevent excessive burning and oxidation during via formation, which will be described in more detail later.

The capacitors are then passivated using a thin Parylene C film. The Parylene is deposited conformally using a room-temperature CVD process. Parylene was chosen due to its well-known moisture barrier properties [74, 75], which limit the absorption of water into the moisture-sensitive, conducting polymer cathode material. The conducting polymer consists of a heterogeneous mixture of PEDOT and PSS. The PSS molecules have a high affinity to water owing to the sulfonate groups, which likely leads to the high rate of moisture absorption [76, 77]. Large degradation in capacitor performance can be attributed to this absorption of moisture, including increased ESR, volumetric swelling, and dielectric corrosion or damage [76-78]. Eventually, moisture can lead to complete component failure. Thus, the passivation layer is critical.

Next, the capacitors are embedded in an epoxy-based material, Ajinomoto build-up film GX92 (ABF GX92), and laminated onto a silicon substrate. The thickness of the epoxy-based build-up material used is 100 μm to ensure complete coverage and planarization of the ~75 μm features that form the thickness of the capacitor above the tantalum carrier foil. The embedding and lamination is performed in vacuum to mitigate any pockets of air that might form. A pressure of 0.3 MPa is applied at a temperature of 130° C for 150 s to achieve complete planarization of the embedded capacitor array, as

this is the temperature at which the build-up material has the lowest viscosity before excessive cross-linking occurs. It is also just above the glass transition temperature of the material. After lamination and planarization, the material is cured at 180° C for 90 minutes.

Electrical access to the capacitor electrodes must then be formed. This is achieved using standard via-formation processes. An ultraviolet (UV) laser is used to first drill vias at the cathode and anode termination sites, and through laser ablation of ABF material, expose the underlying metal surfaces. To optimize the drilling conditions, the relationship between laser power, number of laser pulses (or repetitions), and drill depth was studied (Figure 46). While increasing the number of pulses can help to drill further through the material, the depth begins to saturate beyond a certain number of repetitions. This is attributed to a certain amount of activation energy needed to remove material, which increases along with depth. Not only must the energy transferred from the laser pulse be enough to cause a phase change in the build-up material to the gaseous state, but the molecules must remain in the gaseous state long enough to be sucked out and away from the opening of the drill site. The distance that the molecules must travel before redepositing as a solid becomes longer as the drill depth is increased. Therefore, more thermal energy must be transferred to the molecules for removal from the site, to avoid redisposition at the drill site and saturation of drill depth.

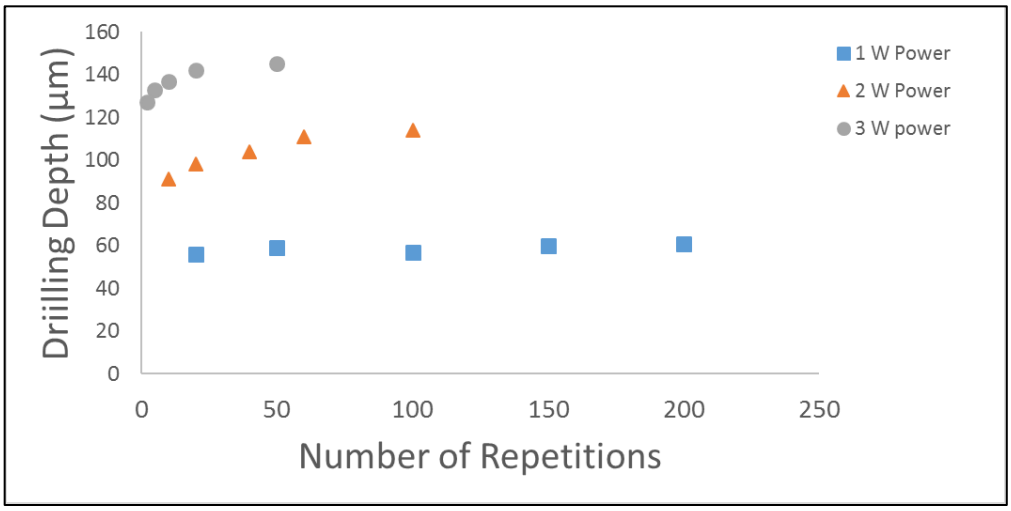
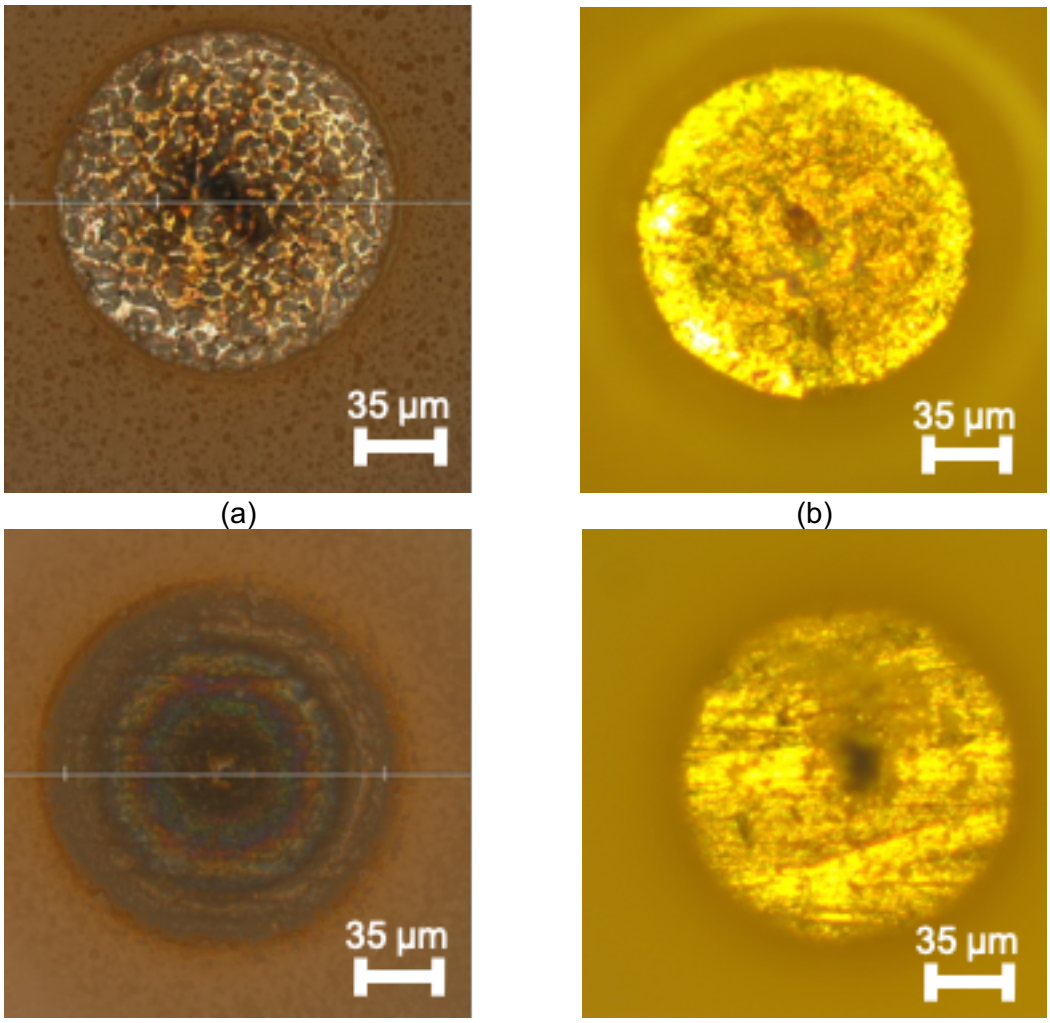


Figure 46. Effect of UV laser power and pulse repetitions on depth of removed build-up material (Ajinomoto ABF GX92) at the drill site

Since the thickness of build-up material is greater above the anode than the cathode, different drilling conditions must be used for each case. It was found that a power of 3 W should be used at the anode sites, while 1 W is sufficient for the cathode. The gold surface finish prevents excessive oxidation of the tantalum anode or burning of the silver paste cathode during laser drilling, which ensures a low-resistance electrical pathway. Here, copper could also be used instead of gold, since a quick acid dip could be used to remove any copper oxides that form. Without the surface finish, tantalum oxide formed at the drill sites to the anode and could not be removed with any sort of chemical or plasma etching techniques. This is attributed to the large enthalpy of oxidation of Ta, which results in a very stable oxide [79, 80]. The difference in levels of oxidation of the underlying metal at the via bottom, whether it be the silver paste cathode or the tantalum foil anode, is very apparent when compared with and without a gold stopping layer (Figure 47).



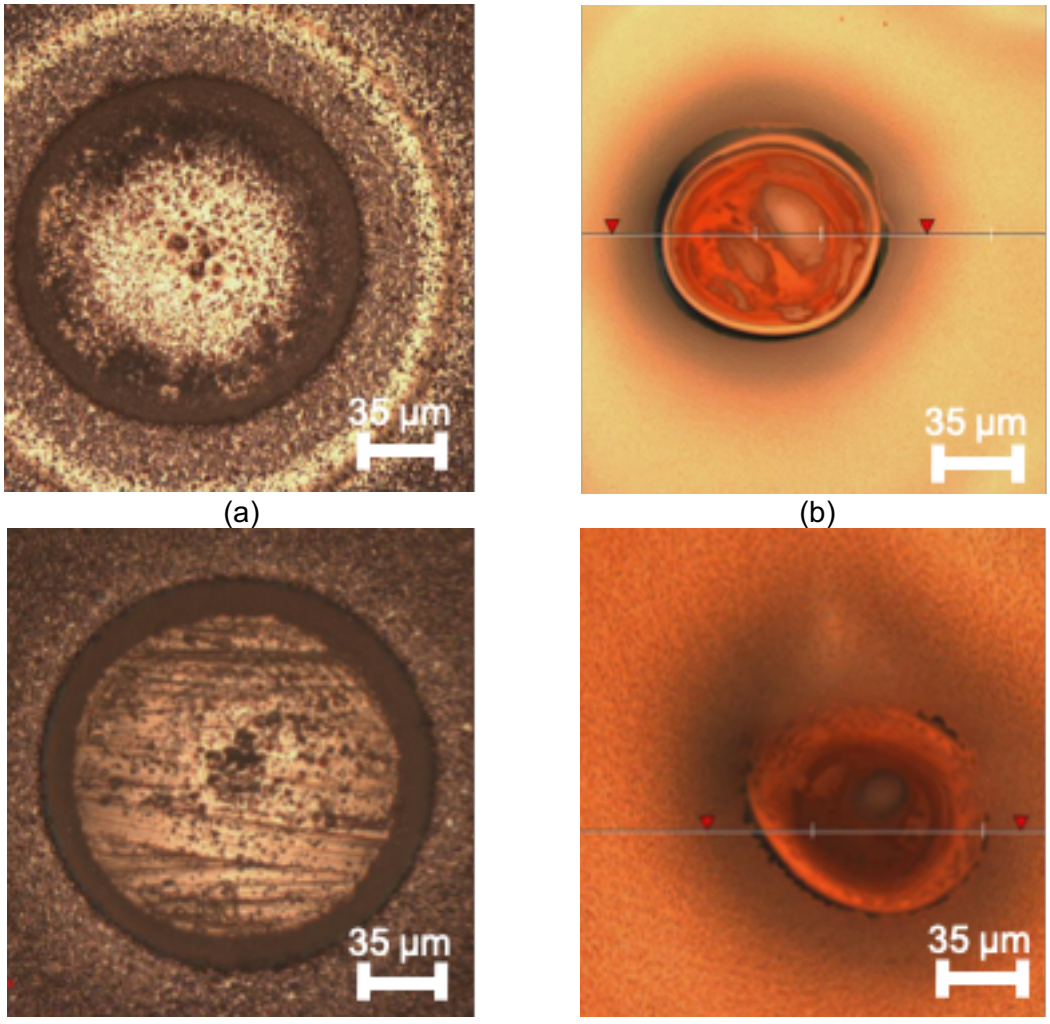
(a) (b)

(c) (d)

Figure 47. Optical images of via bottoms after UV laser drilling for (a) cathode landing without gold stopping layer, with burning of silver paste visible; (b) cathode landing with gold stopping layer; (c) anode landing without gold stopping layer, with tantalum oxidation visible; (d) anode landing with gold stopping layer

After laser drilling, a thin copper (Cu) seed layer is deposited onto the structure. This can be achieved using Cu sputtering or an auto-catalytic chemical (electroless) deposition process, as is shown in Figure 48a and Figure 48c. Here, a 200 nm thick Cu seed-layer is used following a 15 nm thick sputtered titanium (Ti) adhesion layer. Photolithography and electrolytic plating is then used to coat the vias with thick copper while patterning and forming copper pads for soldering connections. Top-view images of the via openings after plating can be seen in Figure 48b and Figure 48d. Finally, the Ti/Cu

seed layer is etched away.



(a) (b)

(c) (d)

Figure 48. Top-view optical images of (a) cathode via opening after copper sputtering (b) cathode via opening after copper electroplating (c) anode via opening after copper sputtering (b) anode via opening after copper electroplating

5.1.2 Electrical Measurements

For capacitance and ESR measurements, an Agilent 4294A Precision Impedance Analyzer is used. The free-standing capacitor array was measured before integration by probing the silver paste cathode layer and tantalum foil anode. After integration, measurements were made by probing the surface of the copper pads, which were

connected to the cathode and anode through the via interconnections.

Leakage measurements were made by charging the capacitors using a constant 1 mA current up to a 3 V bias. Then, the capacitors were kept at a constant voltage of 3 V while the current needed to maintain this bias was monitored. The actual values for the leakage current are taken after 5 minutes at constant voltage, to allow time for the transient current to settle.

5.2 Results and Discussion

A cross-section of an embedded capacitor's multi-layer structure is shown in Figure 49. The bottom layer consists of a solid tantalum carrier foil that is measured to be 28 μm thick. This is thin enough to keep the overall capacitor thickness small while also providing mechanical support during processing and foil-transfer. The foil remains flexible at this thickness, which could potentially be useful in flexible electronics applications. The next layer shown is the porous tantalum layer, which consists of the sintered, partially oxidized, tantalum nanoparticles. The nanoparticles are sintered after printing, creating a high-surface area, porous network that is electrically connected to the carrier foil. The total thickness of this porous portion is ~50 μm.

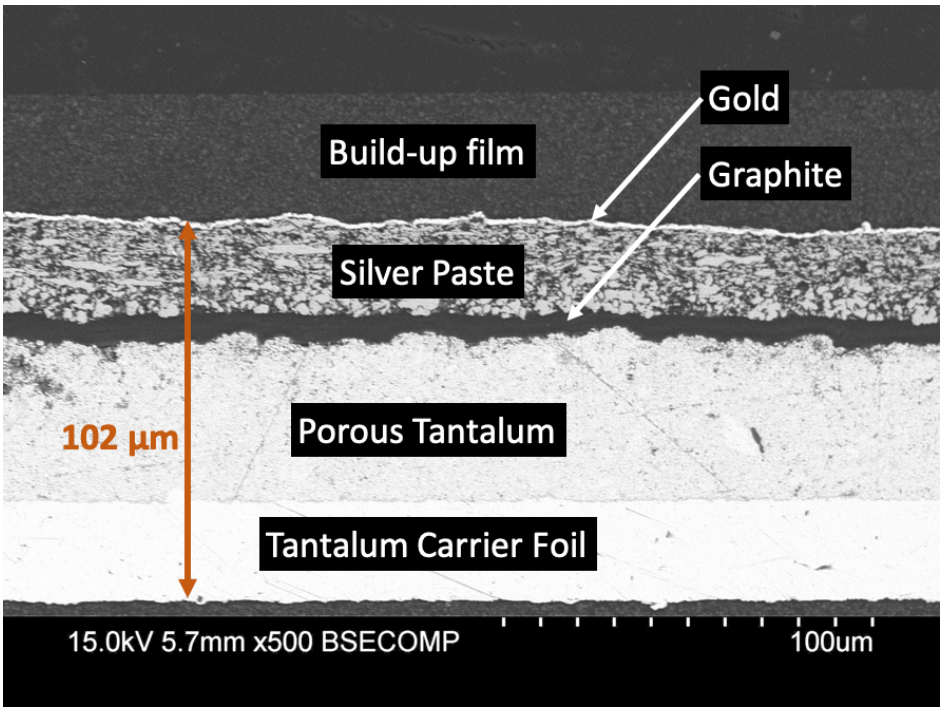


Figure 49. Cross-section of ~100 µm thick tantalum capacitor structure

Coated on the metal-oxide core-shell nanoparticles is the PEDOT:PSS conducting polymer cathode. A final conducting polymer coating is applied on top of the tantalum nanoparticles to improve adhesion and current collection, followed by a graphite layer and silver paste layer. The graphite layer and silver paste layer are 5-10 µm and 20-25 µm, respectively. The total combined thickness of the capacitor structure is shown to be ~100 µm. It is likely that by using a highly-controlled printing process to deposit the graphite and silver paste layers, both the ESR and total thickness of the capacitors could be reduced by using thinner layers here. Additionally, the final gold layer for low contact resistance and reduced burning during laser drilling can be seen. In this case, a thick 450 nm gold layer is used.

Another image of the embedded capacitor cross-section is included in Figure 50a. The silicon substrate can be seen beneath the capacitor, with a thin build-up film that acts as an adhesive between the two. The edge of the capacitor is shown to highlight the level

of planarization achieved using the build-up film. The thickness of the various layers of the capacitor, including the porous tantalum, graphite, and silver paste, are thinner towards the edge of the capacitor, forming a curved convex shape on the foil as expected of a printed viscous paste. However, the total thickness above including the build-up film remains consistent across the entire wafer, thus demonstrating the planarization.

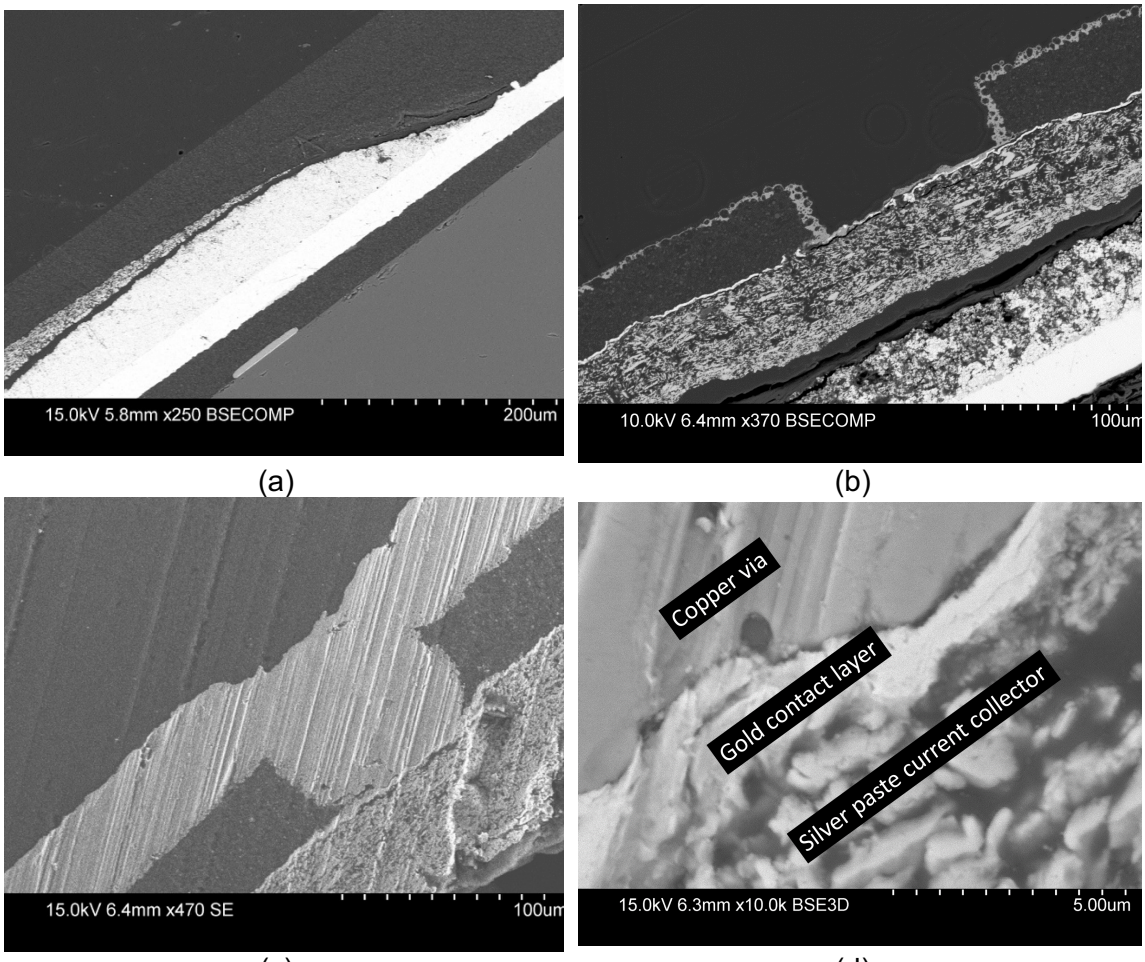
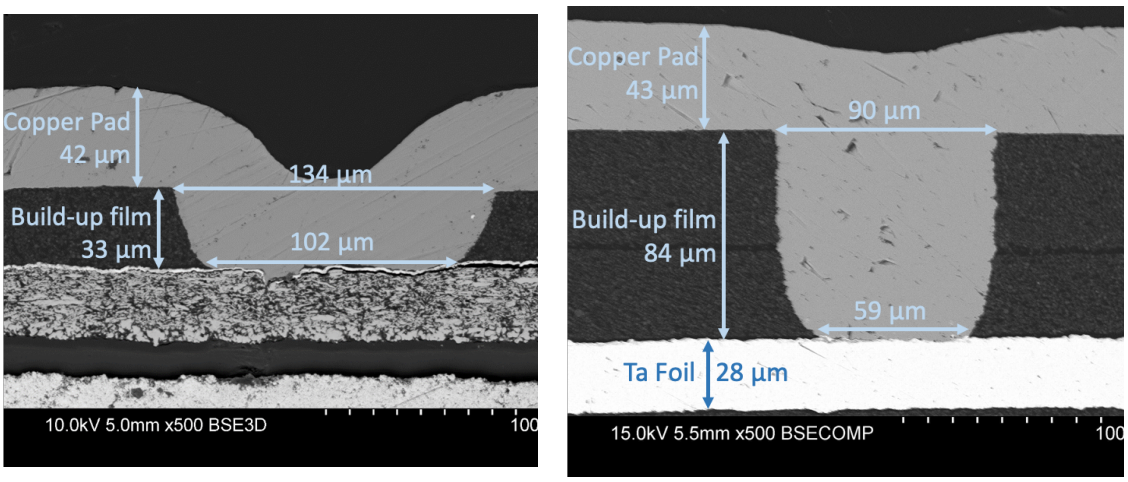


Figure 50. (a) Thin-film Ta capacitor laminated and planarized on silicon (b) Thin-film capacitor after laser drilling of via and electroless copper deposition (c) Partially filled copper via contacting Au/silver paste cathode layers (d) Thin gold layer between copper via and silver paste layer for low resistance electrical connection

Figure 50b shows the capacitor cross-section after laser drilling and auto-catalytic

electroless copper plating. Conformal deposition of the copper seed-layer is observed all along the via bottom and sidewalls, which is important for proper via filling and low-resistance electrical connection. This was achieved using sufficient agitation and vibration in the plating baths. In some cases, copper sputtering was used to deposit the seed layer instead. In the next process steps, the via is galvanically plated to form a conformal coating of thick copper as shown in Figure 50c. Good contact between the copper via and gold contact layer can be seen, with the gold helping to improve the contact resistance between the copper via and silver paste layer (Figure 50d).

A structural comparison between the copper vias forming the anode and cathode interconnections is made in Figure 51. The via to the tantalum carrier foil, and thus the anode, must be much taller due to the build-up film thickness of ~85 µm. This structure shows a high aspect ratio of ~2.7 for the height-to-diameter tapering, or ratio of the height to the difference in diameter between the via opening and via bottom. Again, good contact between the tantalum foil, gold contact layer, and copper via is seen. For the cathode vias, there is only ~35 µm of build-up film to drill through. In this case, the aspect ratio is ~1.



(a) (b)

Figure 51. (a) Copper via interconnection to silver paste current collecting layer, electrically connected to conducting polymer coating on porous tantalum nanoparticles (b) Copper via interconnection to tantalum carrier foil, electrically connected to porous tantalum nanoparticles

The capacitors were electrically tested before and after integration to assess the viability of the process. The capacitance measured across a broad frequency range of 10 kHz to 1 MHz is shown in Figure 52a. The 5 mm^2 capacitors show high density of greater than or roughly equal to 1μF/mm^2 up to 1 MHz, with a 30% drop between 10 kHz and 1 MHz. This frequency stability is well beyond what typical tantalum capacitors are capable of. Again, the improved stability is related to the thin-film architecture of the capacitor that reduces the length of the conduction path for the charge and discharge current. Additionally, the capacitance at 10 kHz before and after embedding and via formation is almost the same, with an average value of 7.07 μF and 6.92 μF respectively.

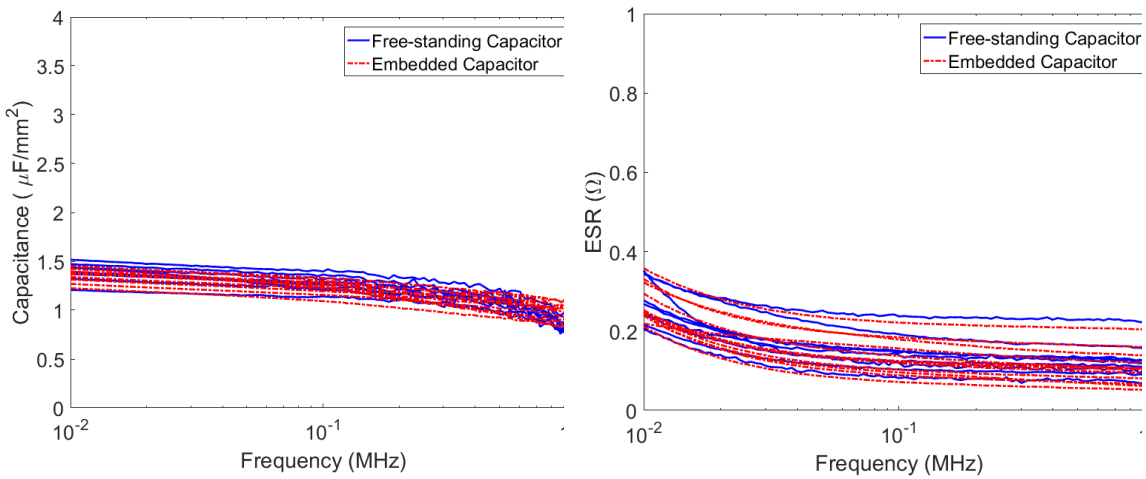


Figure 52. Frequency characteristics of a capacitor array before and after capacitor integration, where the embedded capacitor measurements are taken through the copper vias (a) Capacitance vs. frequency (b) ESR vs. frequency

The ESR was also measured before and after integration, and in both cases, shows a very similar response even though the embedded capacitors are measured through the copper vias (Figure 52). The similarity in measurements indicates low bulk resistance and contact resistance of the copper vias. The average ESR after integration

is just 98 mΩ at 1 MHz, with one capacitor showing as low as 51 mΩ. As capacitors reduce in size and thickness, there are less electrode elements in parallel which results in increased equivalent resistance. Therefore, ultra-thin capacitors typically generally have higher ESR than bulk surface-mounted devices (SMDs). One of the thinnest SMDs available today, with a thickness of 250 μm, shows an ESR of >400 mΩ at 1 MHz [81], so an average ESR of 98 mΩ for the measured tantalum capacitors is quite low.

Additionally, differences in thermal expansion coefficients of the capacitor materials could result in delamination issues or stresses at the polymer-graphite-silver paste interfaces due to the many different temperatures used during processing. Delamination could lead to increased contact resistance between layers and higher ESR. However, this does not appear to be the case here. In some of the capacitors, the ESR actually improves after integration, which is attributed to a reduced resistance contribution from the conducting polymer or current collector layers that make up the cathode. One possibility is there could be some thermally-induced rearrangement of the PEDOT chains within the conducting polymer mixture that leads to a higher conductivity. Alternatively, the graphite or silver pastes may become more cross-linked as the high-temperature integration processes cause further curing, which may lead to a higher conductivity in one or both layers. The reduced ESR also causes a smaller RC constant, and is the reason for the slightly improved frequency stability or reduced roll-off observed in the capacitors after embedding. The average capacitance at 1 MHz is seen to increase from 4.29 μF to 4.82 μF.

Finally, with only a distance of 100 μm between the anode and cathode terminals, and the use of copper vias to form the interconnects, the inductance loop of the capacitor is kept quite small. The inductance loop between terminals is usually what dominates the equivalent series inductance (ESL) of a capacitor, so the ESL of these capacitors is expected to be quite small, although it is not measured.

The capacitor leakage was also measured before and after embedding and via formation. With all the processing and handling that exists in the integration process, as well as a relatively high pressure applied to the capacitors during the planarization of build-up material (0.3 MPa), it is possible to induce mechanical damage to the sensitive dielectric. Additionally, the high-temperature processing could lead to thermomechanical stresses arising from differences in thermal expansion of the capacitor materials, especially at the dielectric-polymer interface. These stresses could lead to dielectric damage and thus increased leakage. Figure 53 shows the distribution of leakage currents in many capacitors before and after processing. The free-standing capacitors showed a very wide distribution of leakage currents, with a mean leakage value of 45.56 μA. After integration, the mean leakage value increased to 80.04 μA. However, much of this was due to an increase in the distribution of leakage current values after integration, with the capacitors that were already showing lower leakage improving but the ones showing high values getting much worse. Some of the already existing microstructural defects in the dielectric were likely further aggravated due to the thermomechanical stresses or chemical absorption processes, but others were unaffected or healed by the thermal processes involved during integration. While the leakage currents are fairly low, they should be improved further to keep the losses in the capacitor as low as possible. Additional processing steps can be added after integration to attempt to heal the capacitor and reduce leakage current. These additional steps will be discussed in RELIABILITY EVALUATION AND MATERIAL COMPATIBILITY STUDY. Thus, the viability of the integration process is demonstrated.

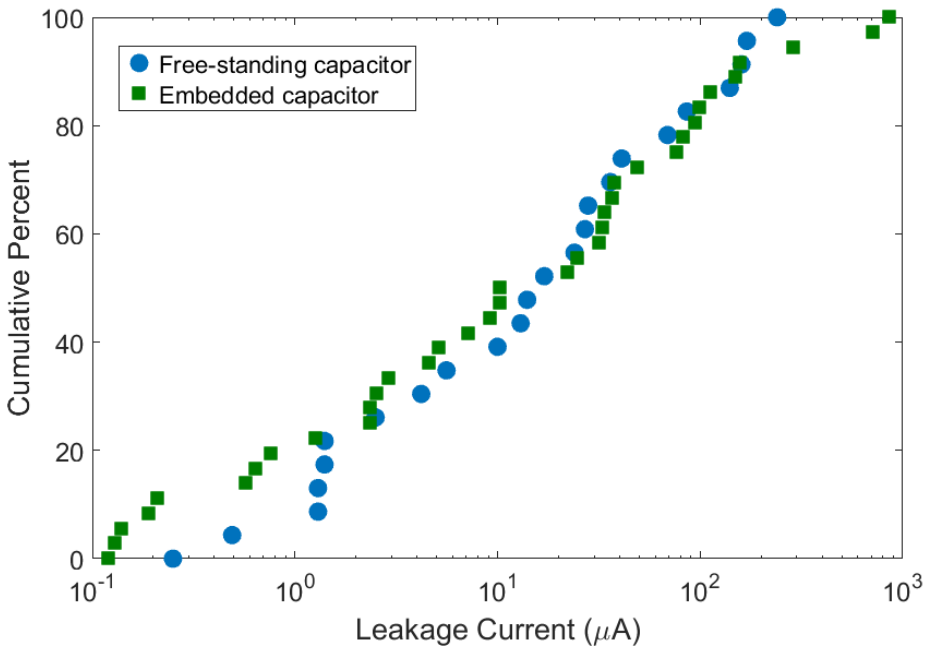


Figure 53. Distribution of leakage currents taken from a total of three separate arrays of ~10 µF capacitors

5.3 Summary

In conclusion, processes such as thin-film lamination, laser ablation, and lithography were used for the package-level integration of ultra-thin tantalum capacitors with high frequency stability and high capacitance density. Through these processes, low-permittivity dielectrics and low-resistance copper interconnects could be carefully deposited around the capacitor to form the package, and thus provide a low-impedance pathway for power conversion and delivery. The capacitors retained a density of ~1 µF/mm^2 at 1 MHz with a thickness of only ~100 µm after integration. The fully integrated capacitors show similar leakage current before and after integration, with some leakage currents being reduced and other being increased due to a combination of damage and healing taking place during the thermomechanical processing steps. The embedded

capacitors can be used for next-generation, miniaturized power delivery systems where high-density passive components need to be integrated close to the switch.

CHAPTER 6: RELIABILITY EVALUATION AND MATERIAL COMPATIBILITY STUDY

The objective of this chapter is to develop a barrier layer material strategy to improve the high-temperature operating capability of the capacitors up to 125° C. Capacitors have been designed and demonstrated that meet the research objectives of high volumetric capacitance density, low ESR, and high frequency stability in an ultra-thin structure with 3D integration capability. However, the reliability of the structure still needs to be demonstrated, especially for operation of the capacitors at high temperatures. This is necessary to ensure the longevity of the capacitors operating near high-temperature components such as the active switches and ICs, which is the case in IVRs. Additionally, the capacitors must be able to handle high current levels to provide high power densities to the rest of the system, which inherently will result in resistive heating.

To meet the objective of high-temperature operating capability, the mechanisms for high-temperature degradation of the capacitors must first be understood. The materials within the capacitor structure were already chosen partially for their stability beyond 125° C. Most notably, the tantalum pentoxide dielectric retains stable permittivity and structure, unlike ferroelectrics [23, 24, 46, 51, 52, 66, 79]. Additionally, the other capacitor materials are also stable up to and beyond 125° C, including the conducting polymer cathode material [76].

At the same time, there are certain aspects of the material system, such as charge conduction through the dielectric and diffusion of foreign species through the various materials in the system, that are accelerated by temperature and can negatively affect capacitor performance. Normally, tantalum capacitors are protected by a molding and casing or metal sleeve, which limits the diffusion of oxygen and moisture into the system. Since the capacitors in this work do not have such a casing, as they are meant for lamination and 3D integration directly on-package, it is critical that the reliability of the capacitors is studied. This chapter will evaluate the reliability of the thin-film tantalum capacitors, both before and after embedding of the structure in epoxy-based build-up material. Parylene C will be introduced as a thin-film barrier material to limit the diffusion of oxygen and moisture into the capacitor structure, and its effect on capacitor reliability will be studied.

6.1 Possible Degradation Mechanisms in Capacitor Materials

There are many possible ways in which tantalum capacitors can degrade over time, especially at high temperatures. The copper interconnections can form copper oxides or hydroxides in the presence of moisture that add resistance and can eventually form bridges that act as electrical pathways between the anode and cathode. Not only this, but positively charged copper ions and silver ions from the silver paste termination layer can migrate into the negatively charged cathode. Enough electromigration can eventually lead to absorption of these ions at the electrode-dielectric interface that increase charge absorption losses and add to the leakage current through the creation of defects in the tantalum pentoxide. Additionally, temperature changes can lead to delamination between cathode interfaces due to difference coefficients of thermal expansion (CTEs).

Most commonly, tantalum polymer capacitors are known to degrade through the diffusion and electromigration of oxygen and water molecules [82, 83]. It is thought that some moisture is good for the capacitor's lifetime and performance, but too much or too little can lead to degradation over time. Due to this, some of the most difficult reliability qualification tests for harsh environments, such as automotive applications, involve high-temperatures in air or high-humidity environments (Table 8). The conducting polymer cathode is composed of polystyrene sulfonate groups, which are necessary to create a viscous suspension of the polymer during cathode deposition. These PSS groups have a high affinity for water due to the charged sulfonate groups. Thus, the cathode material is susceptible to moisture-induced degradation, which is accelerated at higher temperatures due to the diffusion of moisture [76-78]. The mechanism for degradation is not entirely understood, but there are several theories, including a reduction in conductivity caused by increased separation between PEDOT domains, and volumetric swelling leading to damage of the dielectric (Figure 54). Additionally, it is possible that the water hydroxyl groups may react with oxidants still present in the cathode and form acids, which may corrode the dielectric or affect the charge absorption at the dielectric-electrode interface [84, 85]. Finally, expansion of the material can aid in the delamination between interfaces.

Table 8. Ability of tantalum capacitors to pass standard reliability testing methods for automotive qualification using MnO_2 versus polymer as the cathode material

AEC Q-200 Rev D Table of Methods for Tantalum & Ceramic Capacitors			
Stress Test Name	**Conditions**	**MnO_2**	**Poly**
High Temp Exposure (Storage)	125° C, Unbiased, 1000 Hrs	✓	✗
Temperature Cycling	-55° C to 125° C, 1000 Cycles	✓	✓
Biased Humidity	85° C, 85% RH, Biased, 1000 Hrs	✓	✗
Operational Life	125° C, Biased, 1000 Hrs	✓	✗
Resistance to Solvents	Mil-Std-202, Meth. 215	✓	✓
Mechanical Shock	Mil-Std-202, Meth. 213, Cond F	✓	✓
Vibration	Mil-Std-202, Meth. 208, 5G's-20min	✓	✓
Resistance to Soldering Heat	Mil-Std-202, Meth. 210, Cond D	✓	✓
ESD	AEC-Q200- 002 or ISO/DIS 10605	✓	✓
Solderability	J-STD-002	✓	✓
Terminal Strength	AEC Q200-006	✓	✓

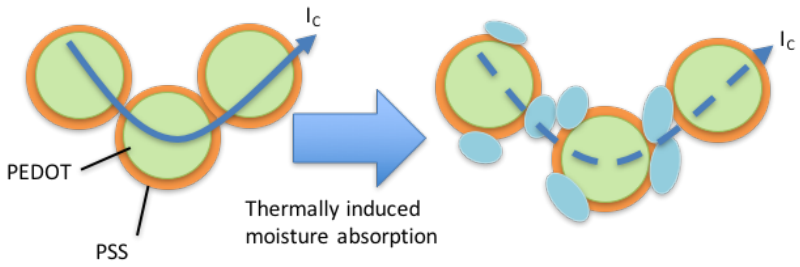


Figure 54. Depiction of the swelling of PEDOT:PSS cathode material caused by moisture absorption, leading to increased resistance and possible damage to the capacitor dielectric material

In terms of capacitor performance, these moisture-induced degradation mechanisms can be summarized into three main categories (Figure 56). Moisture leads to swelling of the conducting polymer. Since the tantalum nanoparticles are not completely covered by conducting polymer (only 80-95% covered), this means that the coverage can increase as moisture is absorbed. That leads to higher capacitance at lower frequencies. However, increased resistivity in the cathode itself, or expansion-induced delamination of the silver or graphite layers, will lead to higher capacitor ESR as

well as higher RC constants. This means the capacitor will begin to roll-off at lower frequencies, and thus have lower capacitance at higher frequencies.

At the same time, the swelling can mechanically damage the Ta_2O_5 dielectric, especially when one considers the difference in CTEs between the polymer and dielectric. Not only this, but the presence of moisture may accelerate the formation of oxygen vacancies in the dielectric, or absorption of foreign species from the cathode, leading to defect sites that act as electron traps and aid in the transport of charge across the dielectric. All of this results in more conduction losses through the dielectric material, increased I^2R heating, and eventual dielectric breakdown.

Finally, the presence of moisture at the dielectric interface can cause changes in the band gap offset between the cathode and dielectric. This may lead to larger charge absorption losses and effectively a higher dissipation factor in the capacitor. Therefore, it is critical to prevent the infiltration of moisture into the cathode material.

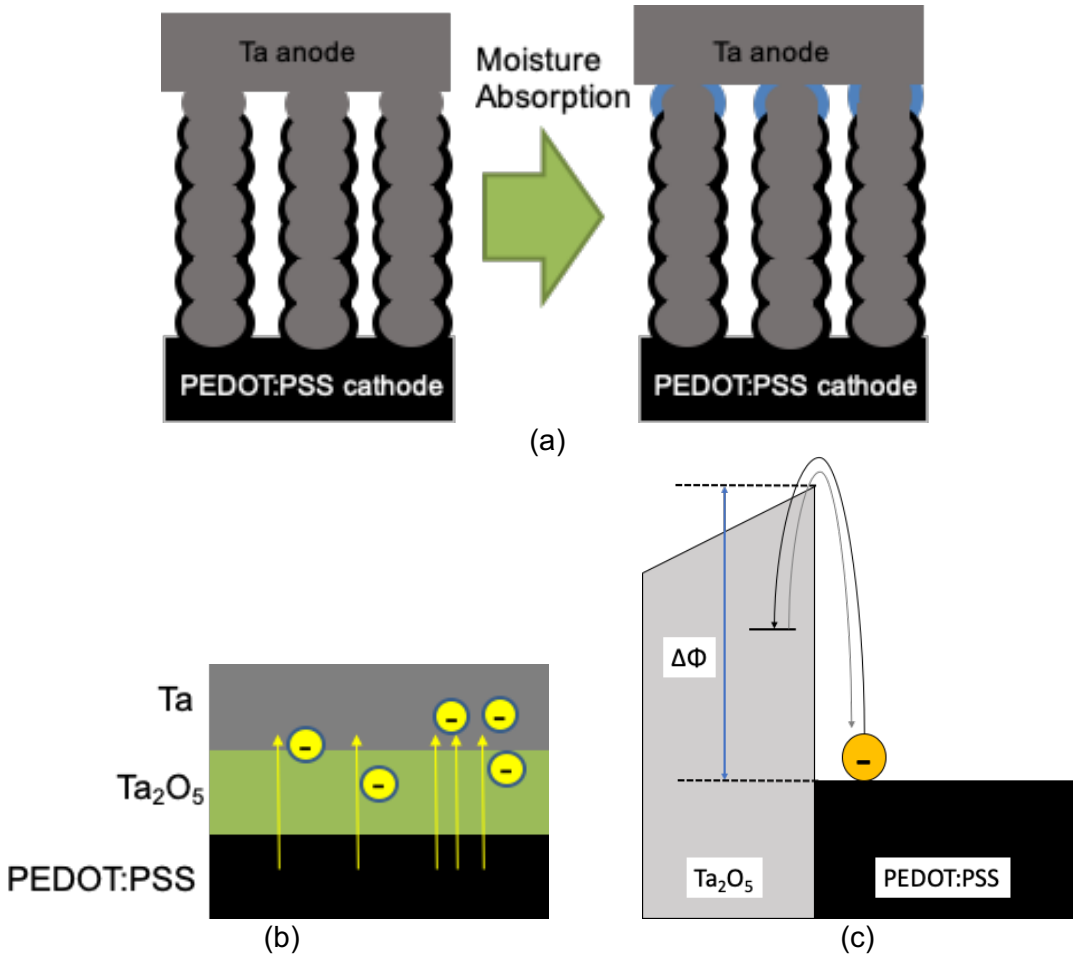


Figure 55. Schematics of how moisture absorption can lead to tantalum capacitor performance degradation including (a) increased capacitance at low frequencies due to increased area coverage of the tantalum nanoparticles but lower capacitance at higher frequencies due to increased resistance, leading to higher RC constants and larger roll-off (b) Increased conduction through the dielectric due to the accumulation and increased number of defects and (c) increased charge absorption losses from changes in band offset energy at the polymer-dielectric interface

In summary, the high-temperature lifetime of the capacitors is limited. Some of the most likely possible degradation mechanisms of the tantalum capacitors is presented in Figure 56. Despite these limitations, recently tantalum-polymer capacitors have been rated for temperatures up to 125° C, achieved primarily by improvements in the packaging of the system that slow the movement of moisture or air into the conducting polymer The last part of this research will focus on developing barrier layer materials to

prevent the diffusion of moisture into the capacitor cathode and push the capacitor reliability into higher temperature regimes, despite the absence of traditional packaging methods. Parylene C is chosen as a barrier layer material due to its well-known moisture and oxygen barrier properties, as well as its ability to be processed as highly conformal thin-films using CVD [74, 75, 86, 87]. The materials will be exposed to high temperatures and humidity levels over an extended period to demonstrate material reliability, and a combination of electrical measurements and imaging will be used to determine failure mechanisms.

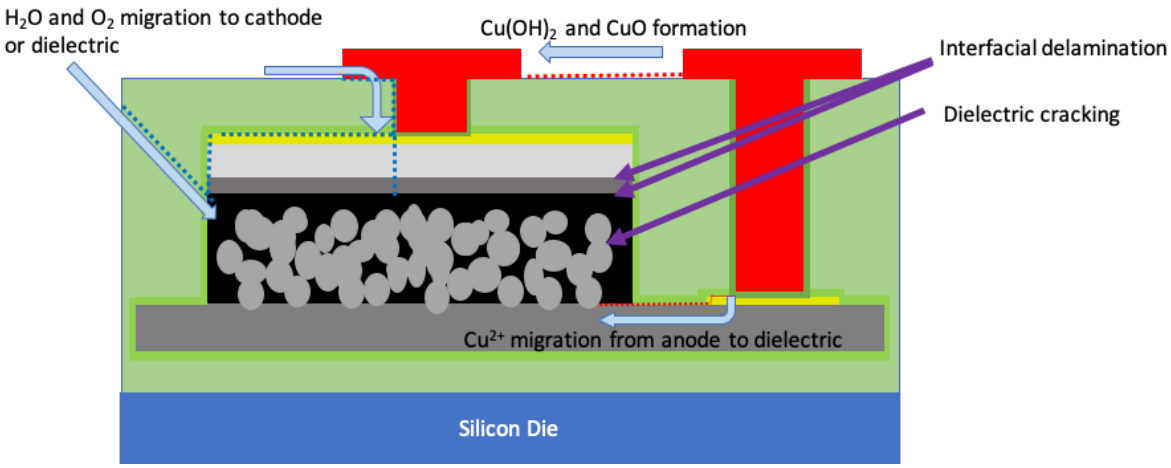


Figure 56. Summary of possible degradation mechanisms in tantalum-polymer thin-film capacitors

6.2 Evaluation and Testing Methods

To test the effect of moisture and air on PEDOT:PSS, a simple test structure was fabricated. The structure consisted of evaporated Cr/Au pads on a glass slide, with printed PEDOT:PSS bridges connecting two pads together. A schematic of the test structure is shown in Figure 57. Multiple bridges were made on a given sample to improve statistical confidence, and many test structures were made for the various tests. Some of the test

structures were then coated in Parylene C using CVD, in thickness ranging from 200 nm to 1000 nm.

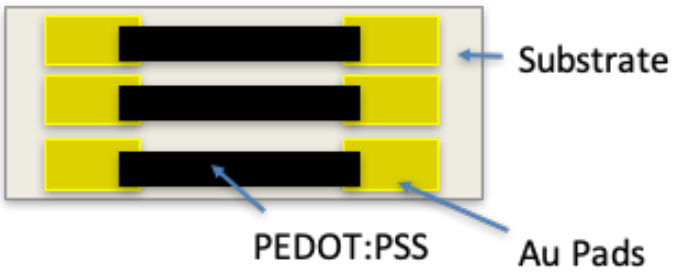
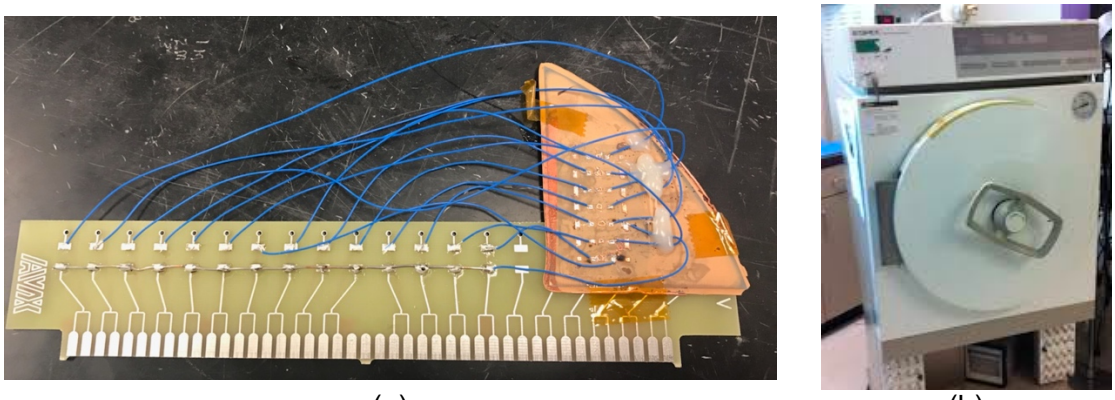


Figure 57. PEDOT:PSS bridges used as test structure to study the effects of moisture and air on PEDOT:PSS morphology and electrical properties

In the first test, the resistance of the PEDOT:PSS bridges were measured before placing the structures in a thermal chamber exposed to air and set at 120° C. The samples were then removed after various intervals of time and the resistance was remeasured. For the samples coated in Parylene C, small areas above the gold pads, where PEDOT was not present, were mechanically removed using acetone, so that the resistance could be measured without interference from the Parylene C.

In another test, the test structures were exposed to a highly accelerated stress test (HAST) chamber, with temperature and humidity control. The chamber was kept at 85% relative humidity and 85° C, and samples were again removed at various intervals of time. In this case, Parylene C was not removed above the gold pads until after removal from the chamber, since it was critical to ensure the absence of intentionally-made pinholes in the barrier film. Due to this restraint, new samples were used for each measurement, rather than remeasuring the same sample at each point in time. The average change in resistance for the samples was recorded after 50 hours, 150 hours, 300 hours, and 500 hours.

A similar test was performed using the tantalum thin-film capacitor arrays. The capacitors were fabricated as described previously, electrically characterized in terms of ESR, capacitance, and DF, before being placed in the chamber. Humidity level ranging from 65-85 % relative humidity, as well as temperatures ranging from 85° C to 125° C, were studied. The capacitors were then retested after exposure to the HAST chamber. In some cases, a DC bias (at the expected operating voltage of the capacitors) was also placed across the capacitors to further aid with electromigration of moisture and oxygen. This was only applied to capacitors that had been fully embedded and integrated, as it was necessary to make solder connection to the copper landing pads to apply the DC bias. Wires were soldered to the copper landing pads, and then soldered to a test board, which could then be electrically connected to electrical outlets within the HAST chamber. An example of this set up is included in Figure 58a. A picture of the HAST chamber used is shown in Figure 58b. The effects of extended exposure to DC bias, humidity, and temperature on the capacitor performance could then be studied. Additionally, the effects of Parylene C coating thickness, and whether or not the capacitors were integrated and embedded in epoxy-based molding compound, could also be studied.



(a) (b)

Figure 58. (a) Testing set up used to connect the integrated capacitor arrays to the electrical outlets within the HAST chamber, where all of the capacitors are connected in parallel to an external voltage source (b) A picture of the HAST chamber used in this study

6.3 Results and Discussion

The change in resistance due to high-temperature exposure in air of the PEDOT:PSS bridges is included in Figure 59. The resistance of control sample without any sort of protective barrier film is seen to increase dramatically, even after 20 minutes of exposure to elevated temperatures. On the surface of the sample, blistering begins to occur after 60 minutes. However, the samples that do use a protective barrier coating of Parylene C exhibit very little change in resistance, with < 2 % change even after 400 minutes. Even so, the resistance increase exhibited in the sample with 500 nm thick Parylene coating is greater than the increase seen in the sample with a 1000 nm thick Parylene coating. This simple test demonstrates the barrier properties of the protective polymer film.

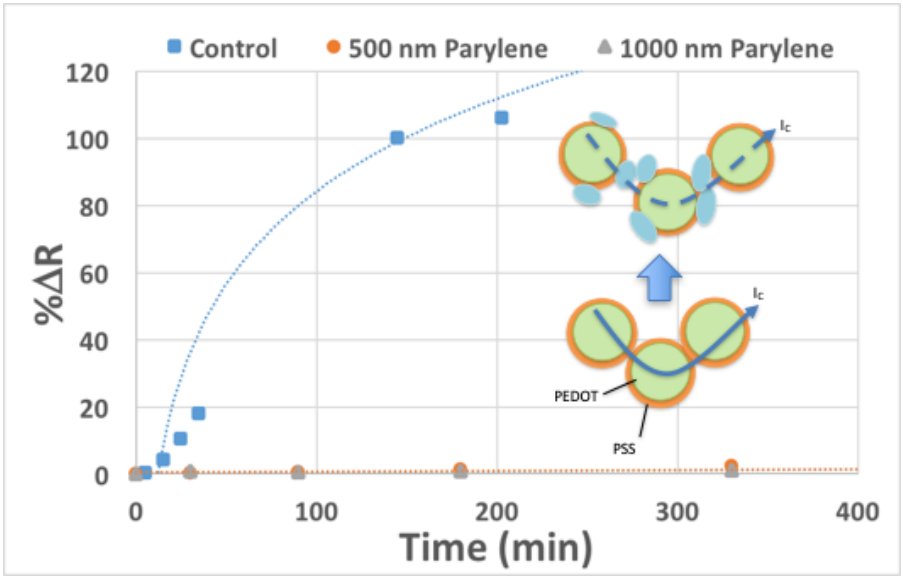


Figure 59. Relative change in resistance of PEDOT:PSS bridges with and without Parylene C barrier coatings after exposure to air at 120° C

Next, PEDOT:PSS bridges were exposed to the HAST chamber at 85°C and 85% relative humidity. Again, the relative changes in resistance of the bridges is recorded in to compare the effect of coating thickness. Those samples with 700 nm thick Parylene C coatings exhibited much smaller changes in resistance than those with thinner coating, even after 500 hours of HAST exposure. In fact, up until ~500 hours, there is actually a reduction in resistance. This indicates some form of annealing or thermally-induced rearrangement of the PEDOT:PSS molecular structure that results in a reduced resistivity, up until enough time is given for moisture to diffuse through the Parylene barrier. Therefore, it is likely that thicker Parylene C coating thicknesses could potentially be used to extend the lifetime of the capacitors in harsh environments such as automotive applications or in IVRs.

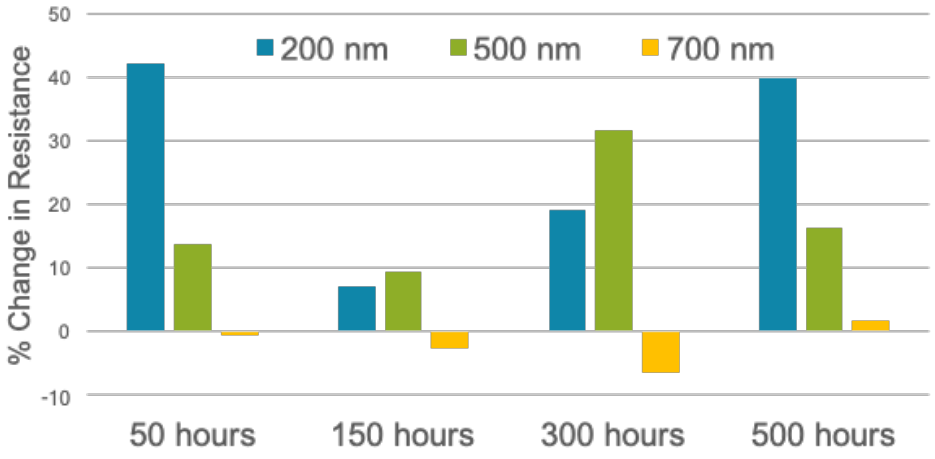


Figure 60. Relative change in resistance of PEDOT:PSS bridges after exposure to 85° C and 85% relative humidity for various periods of time and with various Parylene C coating thicknesses

To study the effectiveness of using Parylene C barriers on the capacitor reliability, sealed capacitor foils were subjected to elevated temperature (65° C) and humidity (95 %

relative humidity) for both 500 and 1000 hours, with 500 hours being a standard test used to rate capacitors up to 105° C. A total of twenty capacitor arrays were used, resulting in over 200 capacitors being tested. The results are summarized in Table 9. The two capacitor arrays tested that used only a 100 nm coating of Parylene had the least number of capacitors passing the HAST, with a pass rate of ~58 %. Additionally, the increase in ESR is observed to increase significantly more on average than the samples with a thicker 200 nm Parylene coating. Those with a thicker barrier layers had a much higher passing rate of 87 %. This demonstrates the capability of using Parylene C as an effective hermetic seal to increase capacitor lifetime and qualify the parts for 105° C operation.

Table 9. Summary of HAST reliability testing results with conditions of 65° C and 95% relative humidity

500 Hours at 65°C and 95% RH					
Capacitor Array # (Parylene C thickness, nm)	**Capacitor Array 1 (100)**	**Capacitor Array 2 (100)**	**Capacitor Array 3 (200)**	**Capacitor Array 4 (200)**	**Capacitor Array 5 (200)**
Average Change in Capacitance (1 kHz)	-0.59 %	+4.46 %	+16.9 %	-8.3 %	+3.19 %
Average Change in ESR (100 kHz)	+934 %	+1295 %	+59.0 %	+103 %	+2.69 %
Fraction of Caps Passing (-20% < ΔC < +30%) (ΔESR < +200%)	7/14	8/12	9/14	9/14	12/14

500 Hours at 65°C and 95% RH					
Capacitor Array # (Parylene C thickness, nm)	**Capacitor Array 6 (200)**	**Capacitor Array 7 (200)**	**Capacitor Array 8 (200)**	**Capacitor Array 9 (200)**	**Capacitor Array 10 (200)**
Average Change in Capacitance (1 kHz)	+5.77	+3.68 %	+4.21 %	-1.02 %	-9.26 %
Average Change in ESR (100 kHz)	+64.9 %	-9.88	-3.25 %	-27.7 %	-40.8 %
Fraction of Caps Passing (-20% < ΔC < +30%) (ΔESR < +200%)	13/14	13/14	8/8	14/14	14/14

1000 Hours at 65°C and 95% RH					
Capacitor Array # (Parylene C thickness, nm)	**Capacitor Array 11 (200)**	**Capacitor Array 12 (200)**	**Capacitor Array 13 (200)**	**Capacitor Array 14 (200)**	**Capacitor Array 15 (200)**
Average Change in Capacitance (1 kHz)	-8.85 %	-6.87 %	-2.3 %	-9.33 %	-19.5%
Average Change in ESR (100 kHz)	+157 %	+221 %	+94.88 %	+37.0 %	+236%
Fraction of Caps Passing (-20% < ΔC < +30%) (ΔESR < +200%)	7/11	9/14	9/14	8/12	10/14

1000 Hours at 65°C and 95% RH					
Capacitor Array # (Parylene C thickness, nm)	**Capacitor Array 16 (200)**	**Capacitor Array 17 (200)**	**Capacitor Array 18 (200)**	**Capacitor Array 19 (200)**	**Capacitor Array 20 (200)**
Average Change in Capacitance (1 kHz)	-11.0 %	-10.4 %	-10.0 %	-8.91 %	-0.725 %
Average Change in ESR (100 kHz)	+193 %	+12.5 %	-11. 69 %	-36.5 %	-55.53 %
Fraction of Caps Passing (-20% < ΔC < +30%) (ΔESR < +200%)	9/11	12/14	13/14	14/14	14/14

Some of the results after 500-hour and 1000-hour exposure are included in Figure 61. Before and after 500 hours, the capacitors shown exhibit consistent capacitance up to 100 kHz with 100% yield. However, a small improvement in frequency stability is also seen after the environmental exposure, resulting in an average ~15% improvement in capacitance density at 1 MHz, from 1.23 $\mu F/mm^2$ to 1.41 $\mu F/mm^2$. The improved frequency stability is attributed to thermal annealing of the conducting polymer resulting in reduced resistivity. This is additionally supported by an observed average drop in ESR of ~27.7% at 100 kHz. Based on these results, it seems the Parylene C can effectively prevent moisture from entering the cathode material. After 1000 hours, a similar change is observed. However, the ESR is improved even further, with an average reduction of ~55.5 % at 100 kHz. The effect can be seen in the improved frequency stability of the capacitance after HAST. The results suggest that as long as excessive moisture is prevented from entering into the system, the performance of the capacitors can actually be improved through extended high-temperature annealing. After HAST, the charge storage ability of the capacitors remains high, with capacitances of >10 $\mu F/mm^3$ at 1 MHz.

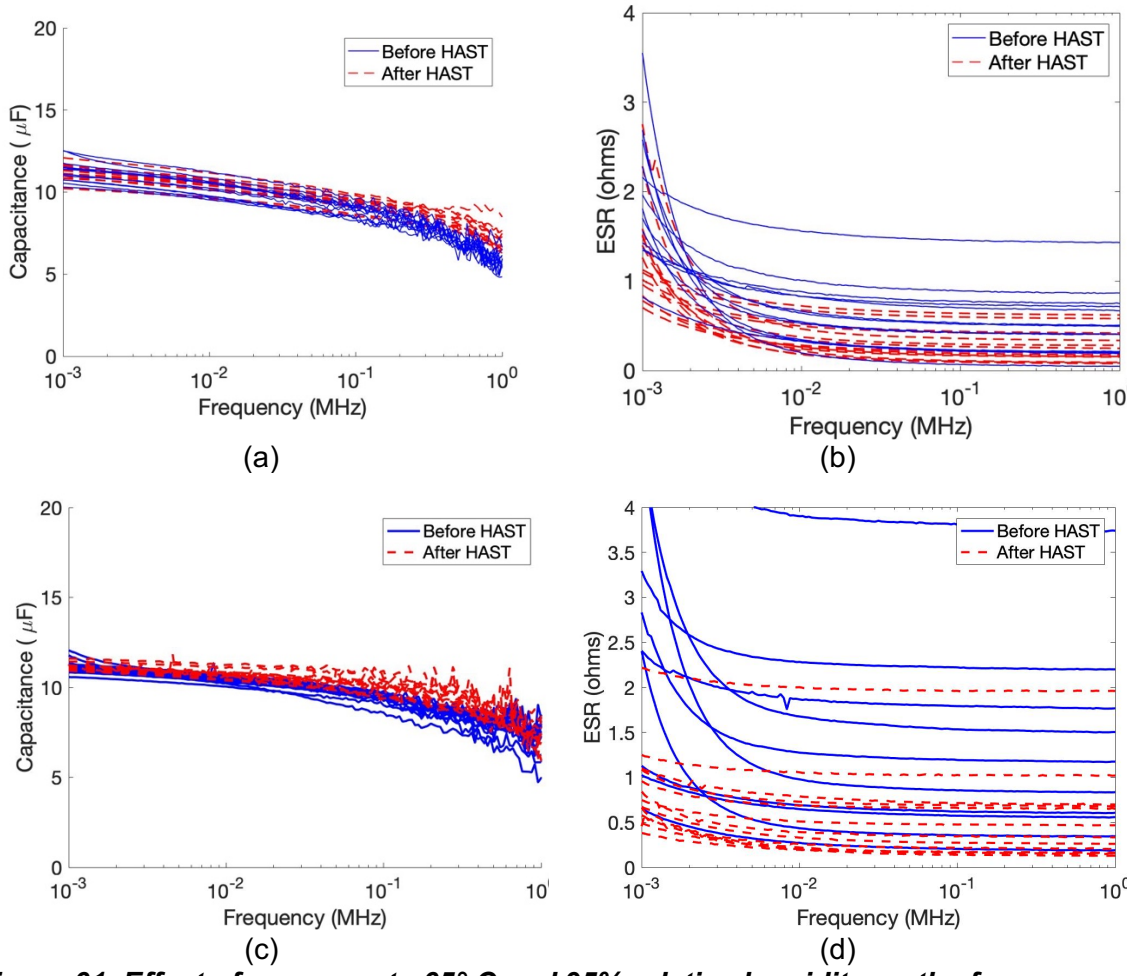
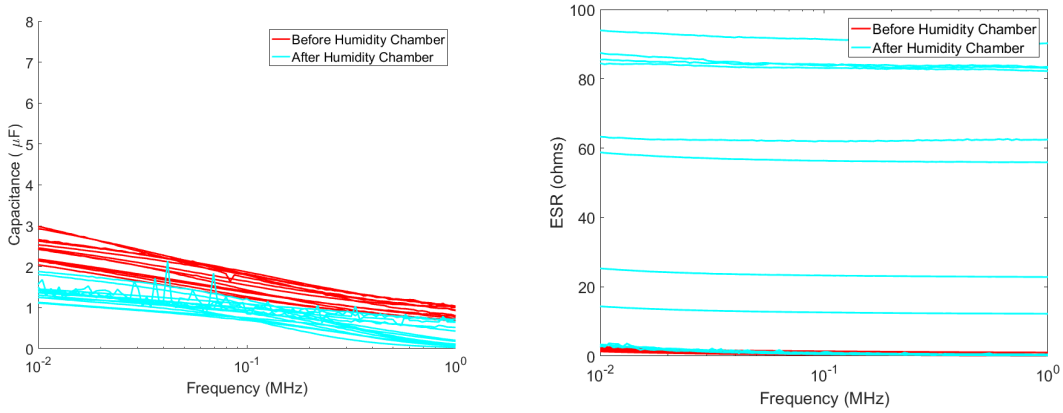


Figure 61. Effect of exposure to 65° C and 95% relative humidity on the frequency response of thin-film tantalum capacitors with a 200 nm Parylene C coating on (a) capacitance, after 500-hour HAST (b) ESR, after 500-hour HAST (c) capacitance, after 500 HAST (d) ESR, after 1000-hour HAST

Capacitors fabricated using the same process and barrier layer coating thickness were also subjected to more extreme reliability testing. In this case, HAST conditions of 125° C and 85% relative humidity were used for 100 hours to force moisture into the system and observe the effects on capacitor performance. Comparing the capacitors' electrical performance before and after HAST shows severe degradation in all cases (Figure 62). There is a huge jump in ESR, from <1 Ω before HAST to >10 Ω in almost all cases, with some capacitors reaching as high as ~90 Ω at 100 kHz. The capacitance is observed to drop at all frequencies above 1 kHz due to the increased roll-off. As predicted

by the PEDOT:PSS bridge tests, 200 nm is not sufficient to protect the capacitors from moisture- and temperature-induced degradation, at least for higher temperatures. Since diffusion is an Arrhenius process, the reduced lifetime of the capacitors is expected for a higher temperature environment.



(a) (b)

Figure 62. Effect of extreme moisture absorption and oxidation on tantalum thin-film capacitors exposed to 85 % relative humidity and 125° C temperature for 100 hours on (a) capacitance and (b) ESR

HAST testing of the fully integrated capacitors is necessary to assess their reliability in a real system, including the capacitor interaction with the molding compound and copper via interconnections. Additionally, the molding compound is expected to improve capacitor lifetime by acting as an additional barrier to moisture and oxygen. HAST was performed for 335 hours at a 3.3 V DC bias in a temperature-controlled chamber. The capacitors were held at a temperature 85° C and 85% relative humidity, which is a common procedure for rating tantalum-polymer capacitors at 125° C. This time, however, a thicker Parylene C coating thicknesses of 500-1000 nm were used to further slow the infiltration of oxygen and moisture and also study the effect of barrier coating thickness. The cumulative distribution of ESRs for the tested capacitors before and after HAST

exposure is included in Figure 63. The effect of Parylene coating thickness is evident. With only a 500 nm thick coating, a large increase in ESR is observed in all of the capacitors. However, when a 700 nm coating thickness is used, the ESR increased can be reduced significantly. Finally, with a 1000 nm coating thickness is used, there is actual a significant drop in ESR in all of the capacitors. The drop in ESR is consistent with previous results, suggesting a thermally-induced process leading to lower cathode resistance. The barrier layer thickness-dependent change in ESR indicates a diffusion-based degradation mechanism, which is attributed to the infiltration of moisture into the conducting polymer. This data confirms the hypothesis that thicker Parylene layers can be used to protect the capacitor from moisture-induced degradation and extend the lifetime of the capacitor.

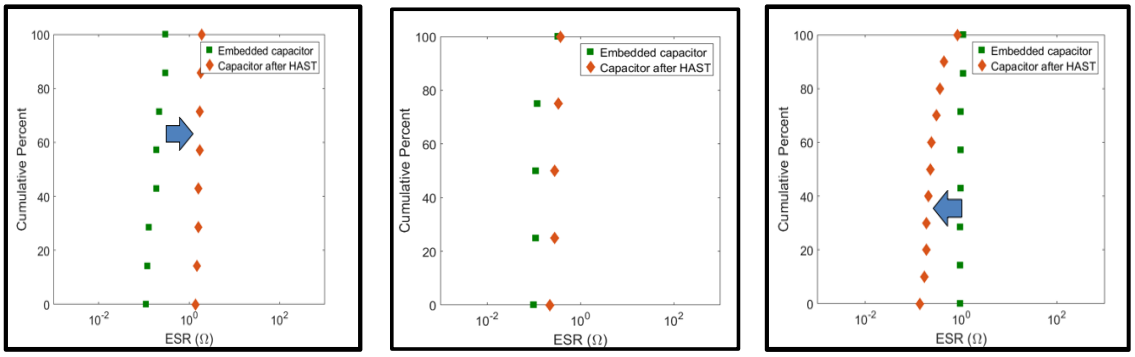


Figure 63. Distribution of ESRs, measured at 100 kHz, from package-integrated capacitors exposed to 85° C, 85% relative humidity, and 3.3 V DC bias for 335 hours where (a) 500 nm thick Parylene C is used, (b) 700 nm thick Parylene C is used, and (d) 1000 nm thick Parylene C is used

While almost all of the capacitors with less than 1000 nm thick Parylene did not pass the HAST testing, almost all of those with the thicker coating did pass. The results are summarized in Table 10. The accepted conditions for passing the test is different for more extreme HAST conditions. In this case, a change in capacitance at 1 kHz of >-5 % but <35 % is considered passing, as well as the requirement that the ESR does not increase by >100 %. Measurements show that 6/8, or 75% of capacitors were able to pass

the 85/85 HAST test when 1000 nm of Parylene C was used. This shows that while more testing should be performed, at least some of the capacitors can potentially be qualified for operation at 125° C.

Table 10. Summary of reliability testing results of capacitors using 1000 nm thick Parylene C barrier layer coating following 335 hours at 85° C, 85% relative humidity, and 3.3 V DC bias

335 Hours at 85°C and 85% RH								
	Capacitor 1	Capacitor 2	Capacitor 3	Capacitor 4	Capacitor 5	Capacitor 6	Capacitor 7	Capacitor Array 8
Change in Capacitance (1 kHz)	+29.2 %	-10.6 %	+26.2 %	-9.52 %	+20.6 %	+25.0 %	+15.9 %	+1.67 %
Change in ESR (100 kHz)	-82.3 %	-87.3 %	-68.0 %	-91.2 %	-55.1 %	-80.8 %	-70.0 %	-80.4 %
Pass/Fail? (-5% < ΔC < +35%) (ΔESR < +200%)	Pass	Fail	Pass	Fail	Pass	Pass	Pass	Pass

Other than the capacitance and ESR, the effect of HAST on the leakage current of the capacitors was also studied. Changes in leakage current can be used to indicate material structural changes in the dielectric. Any degradation of the Ta_2O_5 dielectric will likely result in increased conduction across the oxide. Conversely, healing may result in reduced leakage current. Each capacitor was subjected to 335 hours at 85° C and a 3.3 V bias, with 85% relative humidity. During this period of elevated temperature and DC bias, it is possible for the dielectric to reform in a process known as “burn-in.” Oxygen can be absorbed from the conducting polymer and diffused through the Ta_2O_5 dielectric before combining with oxygen vacancies and healing the defect site. Additionally, the extended time at high temperatures can lead to other types of defect migration and extinction as is the case in any annealing process. The conducting polymer itself also goes through a self-healing process. High local currents are generated at the dielectric defect sites where

charge migrates directly from the cathode to the anode. These currents result in local Joule heating that burn away conducting polymer at the defect sites and thus electrically isolate them from the rest of the capacitor. While the loss to capacitor area from this self-healing process is negligible, the leakage is dramatically reduced.

As can be seen in Figure 64, all the capacitors showed dramatically reduced leakage current after HAST, with the mean leakage value reduced to 122 nA. Removing the single outlier that showed a value of 1.9 μA after burn-in, that mean drops to 71 nA. After burn-in, 80% of the capacitors showed <100 nA leakage current with a mean value of 27 nA. Thus, the better 80% of these ~10 μF capacitor exhibited <10 nA/μF of leakage current after burn-in. The distribution of leakage currents was also dramatically reduced, as seen in the reduced slope of the cumulative distribution function.

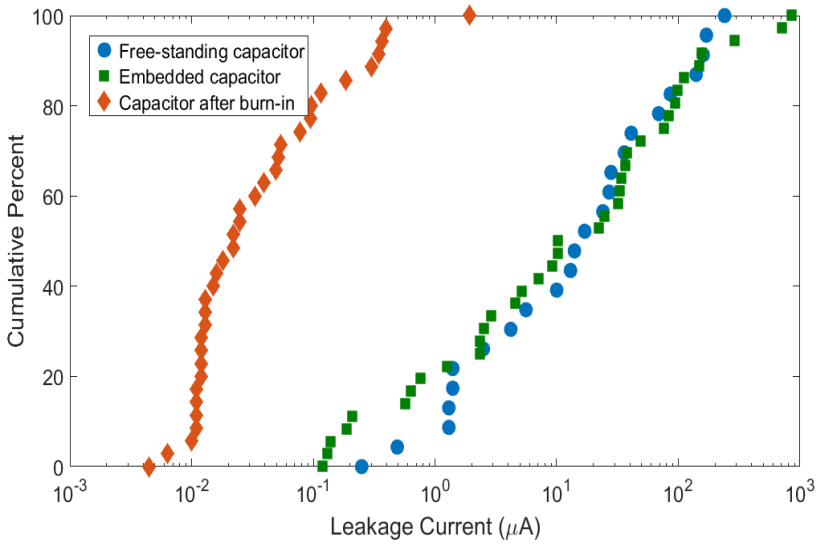


Figure 64. Cumulative distribution of leakage currents for tantalum thin-film capacitors after fabrication (free-standing), after integration and via formation (embedded), and 335 hours of HAST at 3.3 V DC bias, 85° C, and 85% relative humidity (after burn-in)

6.4 Summary

In summary, the reliability of the thin-film capacitor structure at elevated temperatures was studied. Moisture absorption and oxidation of the PEDOT:PSS cathode material was identified as the degradation mechanism that the capacitors were most susceptible to. Moisture and oxidation result in increased resistance in the cathode and increased losses from the dielectric, so a method to limit their diffusion into the capacitor structure was developed. It was shown that vapor-deposited Parylene C coatings can be used to effectively improve the lifetime of capacitors operating at higher temperatures. With a coating thickness of only 200 nm, it was demonstrated that the capacitors could pass 1000 hours of HAST at 65° C and 95 % relative humidity, thereby indicating capability of the capacitors to operate at 105° C. With a coating thickness of 1000 nm, capacitors were able to survive 335 hours at 85° C, 85% relative humidity, and 3.3 V DC bias. This shows potential for the capacitors to operate at 125° C. With high temperature capability, the capacitors can more readily be used in IVR packaging approaches and perform better at higher power density levels, where temperatures are generally much higher.

CHAPTER 7: RESEARCH SUMMARY, CONTRIBUTIONS, AND FUTURE WORK

The objective of this research was to design and demonstrate ultra-thin, 3D package integrated capacitors with ultra-high capacitance density and frequency stability, with low ESR and high temperature stability, so that they could be used in high power-density IVRs. Capacitors based on printed tantalum nanoparticles were proposed as a way to provide a high surface area structure in a thin form factor. Tantalum pentoxide dielectric materials provide high temperature stability and resistance to

degradation, helping to allow for higher current densities while also providing a fairly high permittivity for high capacitance density. Conducting polymer cathodes offer a material capable of infiltrating the nanoporous structure while also offering low resistivity and self-heling for low power losses. All of this leads to IVRs with higher efficiencies and power densities.

7.1 Research Summary

7.1.1 Capacitor Design

A model was developed to correlate the capacitor materials nanostructure to the bulk electrical properties of the device. By using a combination of FEA simulations and circuit analysis, an equivalent circuit could be constructed based on the capacitor materials' structures that could then be used to predict the frequency characteristics of the capacitor including the capacitance density, ESR, and frequency stability. The model was shown to agree well with measurements of a physical tantalum capacitor system. Through modeling, it was predicted that by using an ultra-thin anode structure, the frequency stability of tantalum capacitors could be improved by orders of magnitude while reducing capacitor ESR, which solves the two main drawbacks of tantalum capacitors.

7.1.2 Capacitor Fabrication and Process Development

A process was developed to fabricate the proposed ultra-thin tantalum capacitor structure. A tantalum nanoparticle slurry was printed as a paste on a tantalum carrier foil substrate to form nanoporous regions of only 50 μm in thickness. An oxide was selectively grown directly on the nanoporous regions using a highly controlled, electrochemical anodization process. The resulting Ta_2O_5 shells surrounding the

nanoparticles formed the dielectric material in the capacitor. Then, PEDOT:PSS was deposited around the nanoparticles using a vacuum infiltration process. This conducting polymer provided the cathode of the capacitor. Finally, layers of graphite and silver paste were printed on top to form the current collecting termination layers of the capacitor. The fabricated capacitors were shown to provide ultra-high capacitance density compared to any existing commercial capacitor technology, while also showing vastly improved frequency stability. Volumetric capacitance densities of >10 $\mu F/mm^3$ were measured at frequencies of 1 MHz. High capacitance densities could also be obtained for high-voltage capacitors that used thicker oxide layers and larger nanoparticle sizes. The relationship between process, capacitor material structure, and performance was studied.

7.1.3 Capacitor Integration

After capacitor fabrication, a process was developed to embed the capacitors on-package and form copper via interconnections to enable 3D IVRs. The capacitors are first vacuum laminated onto a package substrate to both embed and planarize the capacitor surface. Access to the capacitor electrodes is achieved using UV laser drilling. Then, copper vias are formed by depositing a copper seed layer, and selectively electroplating copper through photolithographic processes. Finally, the copper seed layer is removed. The capacitors were shown to retain their electrical properties after the integration process, and no noticeable degradation of the capacitor materials or properties was observed.

7.1.4 Reliability Evaluation

Capacitor reliability at high operating temperatures was demonstrated through the use of highly accelerated stress tests. It was shown that Parylene C could be used as an effective barrier layer material to limit the diffusion of harmful species into the capacitor structure, thereby extending their lifetime at high temperatures. Capacitors with 1000 nm of barrier layer material were demonstrated to survive 335 hours at 85% relative humidity, 85° C, and 3.3 V DC bias, indicating their capability for use at high temperatures of 125° C.

7.2 Key Scientific and Engineering Contributions

The contributions from this work can be summarized as follows:

1. A model was created to accurately predict the properties of nanoparticulate capacitors based on their nanostructure, which is increasingly important as higher capacitance densities are needed in smaller form factors. The model shows an improvement in frequency stability can be achieved by reducing the mean path length for the charging and discharging current through the capacitor. Understanding the relationship between electrode nanostructure and bulk device properties can help design future capacitor systems.
2. A process was developed to fabricate capacitor devices that achieve ultra-high capacitance density, low ESR, and frequency stability into the MHz regime all while maintaining a thickness of <100 μm. The process provides good control over the nanoporous tantalum electrode and Ta_2O_5 dielectric nanostructure, and thus the ability to achieve optimal tantalum capacitor material structure for any design need.

3. An innovative process was developed to integrate the capacitors on-package in a 3D approach, which is necessary for future generations of 3D integrated voltage regulators. Through thin-film lamination, laser ablation, and lithographic processes, low-permittivity dielectrics and low-resistance conductors could be carefully deposited to form the package around the capacitor structure and provide a low-impedance pathway for power.
4. A method to improve the high-temperature lifetime of the capacitors was demonstrated by implementing a Parylene C barrier layer film that limits the diffusion of moisture through the capacitor structure, so that the capacitors can be rated for the high temperatures that exist in IVR distribution networks in electronic systems. Understanding the effect of moisture on PEDOT:PSS is an important area of research in materials science not just for capacitors, but in many areas of consumer electronics, power systems, and sensors.

7.3 Future Work

Although demonstration of novel thin-film tantalum capacitors has been completed, there remains some improvements that could further advance the technology. Potential future work can be categorized into three main areas: cathode infiltration process improvement, alternative cathode materials, and continued reliability evaluation.

7.3.1 Cathode Infiltration Process Improvement

Through modeling, it was shown that the frequency stability of the capacitor is limited by the resistance through the capacitor cathode. The cathode material is much thinner and has a higher resistivity than the anode, resulting in high RC time constants

when the capacitor is charging and discharging. With a thick, conformal conducting polymer coating surrounding the tantalum-oxide nanoparticles, frequency stability beyond 10 MHz can be achieved. However, after capacitor fabrication, it was seen that the conducting polymer is not conformally deposited on the nanoparticles, with only 80-90 % coverage achieved. Not only does this slightly reduce the low-frequency capacitance, but it results in areas where the conducting polymer is exceptionally thin. Thus, there are areas with higher resistance that dominate the ESR and frequency stability of the capacitor. Currently, a vacuum infiltration process is used to deposit the conducting polymer, to force the cathode into the nanoporous region. It may be possible to enhance the capillary action of the conducting polymer by reducing the surface tension between the conducting polymer and Ta_2O_5. For example, a siloxane treatment, or something that can add more polar groups to the tantalum pentoxide surface, may be able to improve its affinity with PEDOT:PSS.

7.3.2 Alternative Cathode Materials

Even with improved deposition of the conducting polymer, the resistivity of the material is still limited when compared to metals. Thus, the ESR and frequency stability of the capacitor is still limited. Titanium nitride offers an alternative cathode material that can be vapor-deposited with the use of ALD and has a much lower resistivity compared to PEDOT:PSS. Additionally, since the material is vapor-deposited in a surface-reaction limited process, long cycle times can be used to access hard-to-reach areas within the nanoporous structure. In this way, very uniform deposition can be achieved. Through modeling, it was shown that this type of cathode material deposited in thickness > 20 nm could allow for capacitor frequency stability until upwards of 100 MHz. In this way, power densities of IVRs could be increased dramatically.

7.3.3 Continued Reliability Evaluation

Finally, initial reliability tests showed that barrier layer materials can be added to the embedded capacitor material system to limit diffusion of oxygen and moisture and improve the high-temperature lifetime of the capacitor. However, there are other tests that would still need to be performed to completely qualify the parts for 125° C operation, including the high-temperature life test, where the capacitors are biased for 1000 hours at 125° C in air, and the temperature cycling test, where the thermomechanical stability of the material interfaces can be evaluated. This would be especially important in this type of capacitor integration approach, where the capacitor is actually embedded in the package rather than surface-mounted on it. Additionally, while results have shown evidence that moisture is the main cause of capacitor degradation during HAST, an analysis of the conducting polymer and dielectric microstructure could reveal more information on the mechanism of degradation on the nanoscopic level.

7.4 Publications

The research outcomes of this work and other activities related to the fulfillment of this PhD has resulted in the following publications.

7.4.1 Peer-Reviewed Journals

1. Spurney, R. G., Sharma, H., Pulugurtha, M. R., Tummala, R., Lollis, N., Weaver, M., Gandhi, S., Romig, M., Brumm, H. (2018). “Ultra-High Density, Thin-Film Tantalum Capacitors with Improved Frequency Characteristics for MHz Switching Power Converters.” *Journal of Electronic Materials*, *47*(9), 5632-5639.

2. Spurney, R. G., Sharma, H., Pulugurtha, R., Tummala, R., Lollis, N., Weaver, M., Gandhi, S., Romig, M., Brumm, H. (2019). “3D Packaging and Integration of High-Density Tantalum Capacitors on Silicon.” *IEEE Transactions on Components, Packaging and Manufacturing Technology*.
3. Spurney, R. G., Sharma, H., Pulugurtha, R., Tummala, R., Lollis, N., Weaver, M., Gandhi, S., Romig, M., Brumm, H. (2019). “Modeling and Validation of ESR and Frequency-Stability of High-Density Nanostructured Capacitors in Embedded Power Converters.” *Submitted*.

7.4.2 Conference Proceedings

1. Spurney, R.G., Pulugurtha, R., Tummala, R., Lollis, N., Weaver, M., Gandhi, S., Romig, M. “High-Voltage Capacitors for Next-Generation Power Modules in Electric Vehicles,” in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*. 2017.
2. Spurney, R., Pulugurtha, R., Tummala, R., Lollis, N., Weaver, M., Gandhi, S., Romig, M. “Demonstration of Hermetic Sealing on Ultra-Thin, Wafer-Integrated Aluminum-Polymer Capacitors for High-Voltage and High-Temperature Applications,” in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*. 2018.
3. Sun, T., Spurney, R.G., Sharma, H., Raj, P.M., Tummala, R. “3D Packaging with Embedded High-Power-Density Passives for Integrated Voltage Regulators,” in *2019 IEEE 69th Electronic Components and Technology Conference (ECTC)*. 2019.

4. Spurney, R.G., Sharma, H., Raj, P.M., Tummala, R. “Everything You Wanted to Know About Capacitors but Were Afraid to Ask – Embedded Capacitors,” *Presentation at Applied Power Electronics Conference (APEC)*. 2018.

7.4.3 Technical Reports

1. Spurney, R.G., Sharma, H., Raj, P.M., Tummala, R. “Capacitors,” in 3D Power Packaging with Focus on Passive Embedded Components and Substrate Technologies. *Technical Report from Power Sources Manufacturers Association (PSMA).* 2018.

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